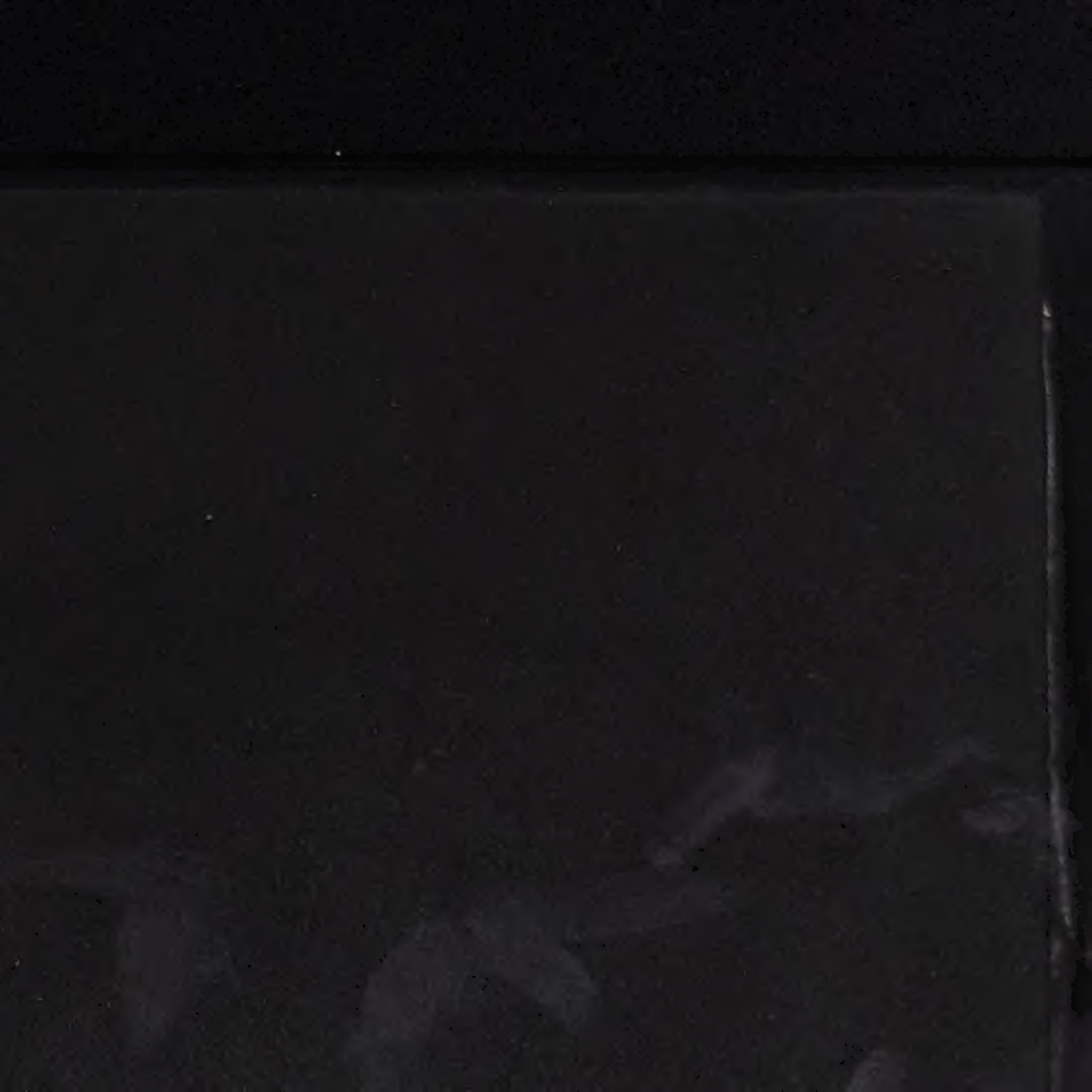

FOREWORD

SCOPE OF INSTRUCTION MANUAL

This manual offers descriptive data and service information for the equipment listed. Service diagrams, parts lists, and printed circuit board details are either a part of this instruction manual, or contained in a supplementary service manual.

NOMENCLATURE

Motorola equipment is specifically identified by the model number on the nameplate.

NOTE

Be sure to use the entire model number when making inquiries about your equipment.

Identifiers have been assigned to chassis and kits. Use these identifiers when requesting information or ordering replacements.

PRODUCTION CHANGES

When production and engineering changes are incorporated into the equipment, a revision number is assigned to the chassis or kit affected; -1, -2, -3, etc.

The chassis number complete with revision number, if any, is stamped on the chassis at the time of production. The revision number becomes an integral part of the chassis identifier. Revisions, if any, are listed on the schematic diagram.

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Changes which occur after an instruction manual is printed are described in the Instruction Manual Revision. These bulletins give the reader complete information on the change including pertinent parts listing data.

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We believe that reports from users provide valuable information for producing good service manuals. Your answers and comments on the following questionnaire will aid us in writing manuals that contain information of maximum benefit to you.

In reference to Manual No. 68P_____

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  _____
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  _____

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  _____
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- ☐ I use troubleshooting charts frequently.
- ☐ I do not use troubleshooting charts.
- ☐ I prefer tabular symptom/remedy charts.
- ☐ The following information should be added (or corrected): _____

  _____

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- ☐ I use the charts to determine content of model or identify what chassis/ kits are in the model; or: _____

  _____
- ☐ I do not use these charts.

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  _____
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MOTOROLA

"MODAX" 100

RADIO PAGING TERMINAL

MODELS E09DAL0100AP
E09DAL0100AC

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TECHNICAL SPECIFICATIONS

Call Capacity	100
Types of Inputs	Rotary Dial Tone Pushbutton
Tone Encoding	Two-Tone Sequential (Tone-Only or Tone-and-Voice -- Standard) Two-Tone Sequential (Subaudible -- Optional)
No. of Transmitters Controlled	1
Types of Transmitter Control	Contact Closure (Local)
Lockout Control	1 Contact Closure (Input and Output)
Automatic Station Identification	Tape Player (Voice)
Number of Tones	10
Frequency Range	67.0 Hz to 1433.4 Hz
Frequency Stability	±.01% (Crystal Controlled)
Frequency Accuracy	±.1%
Output Amplitude	Adjustable to +2 dBm into 600Ω
Receive Audio Sensitivity	-8 dBm minimum
Adjustable Audio Signals	Transmit Audio
De-emphasis	6 dB/Octave, 300 Hz to 3000 Hz
PABX Interface Unit	Bell System Voice Connecting Arrangement DCK/DCL and/or DCW or Equivalent
Number Interchange and Invalidation	Universal Number Interchange: All pager numbers
Power Input Requirements	115 V ac ±10%, 60 Hz/13.8 V dc @ 1 ampere
Operating Temperature Range	32°F to 120°F (0°C to 50°C)
Cabinet Dimensions	16 Inches Wide by 14 Inches Deep by 5-1/4 Inches High
Weight	Less than 22 lbs. (10 kg.)

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Printed in U.S.A. 11/24/78

MODEL/OPTION CHART

FOR

"MODAX" 100

RADIO PAGING TERMINALS

CODE:

[1] [2] = NUMBER OF ITEMS SUPPLIED

[O] = ITEM OMITTED

[A] = ACCESSORY ITEM

ITEM	DESCRIPTION	MODEL/OPTION	E09DAL0100AP	E09DAL0100AC			R076AA	R077AA	R078AA	R079AA	R080AA	R081AA	R019AC	R148AA	R166AA	R167AA	R175AA
	DESCRIPTION		RADIO PAGING TERMINAL	RADIO PAGING TERMINAL/TWO-WAY	FACTORY INSTALLED OPTIONS		LINE LEVEL INPUT (DIAL)	LINE LEVEL INPUT (TONE)	SELECTOR LEVEL INPUT (TONE)	EMERGENCY PAGE	DELETE UNIVERSAL NUMBER INTERCHANGE (UNI)	230 VAC, 50 Hz OPERATION	DELETE AUTOMATIC STATION IDENTIFICATION (ASI)	DELETE ASI TAPE CARTRIDGE	SUBAUDIBLE FILTER	TONE-ONLY, BATTERY SAVER	TONE-ONLY, FAST TIMING
NLN5108A	MAIN CIRCUIT BOARD (WITHOUT EMERGENCY PAGE)		1	1						O							
NLN4482A	CODE PLAN ROM		2	2													
NLN5111A	INPUT BOARD, SELECTOR LEVEL (DIAL)		1	1			O	O	O								
NLN5115A	UNI PRIMARY BOARD		1	1							O						
NLN5116A	UNI DISPLAY PANEL AND BOARD		1	1							O						
NLN5107A	ASI ASSEMBLY		1	1								O	O				
NLN5049A	ASI TAPE CARTRIDGE		1	1								O	O				
NHN6305A	HOUSING AND CHASSIS ASSEMBLY		1	1										O			
NLN5117A	IDENTIFICATION PLATE		1	1													
NBN6111A	PACKING KIT		1	1													
NLN4534A	LABEL, CODING		1	1													
NLN5110A	INPUT BOARD, LINE LEVEL (DIAL)						1										
NLN5112A	INPUT BOARD, LINE LEVEL (TONE)							1									
NLN5113A	INPUT BOARD, SELECTOR LEVEL (TONE)								1								
NLN5109A	MAIN CIRCUIT BOARD (WITH EMERGENCY PAGE)									1							
NLN5118A	BLANK PANEL, FRONT										1						
NLN5114A	LINE LEVEL INTERFACE CIRCUIT						1	1									
NKN6254A	CABLE, TELEPHONE PLUG						1	1									
NKN6256A	CABLE, INTERCONNECT						1	1									
NLN4223A	SERIAL PLATE						1	1									
NLN4484A	SUBAUDIBLE KIT														1		
NLN4485A	BATTERY SAVER TONE-ONLY KIT															1	
NLN4607A	FAST TIMING TONE-ONLY KIT																1
NLN4300A	TWO-WAY BOARD			1													
NLN5119A	19-/23-INCH RACK MOUNTING KIT		A	A													
NKN6255A	RDMZR CABLE		A	A													
TKN6065A	TERMINAL-BASE CABLE		A	A													
NMN6075A	TEST TELEPHONE (DIAL)		A	A													
NMN6076A	TEST TELEPHONE (TONE)		A	A													
NLN1319A	MAXAR INTERFACE KIT		A	A													

EPF-8954-A

NOTES

DESCRIPTION

1. INTRODUCTION

The "MODAX" 100 Paging Terminal is the principal control unit for a telephone-interconnected radio paging system. The paging system provides radio contact with a selected individual or group of individuals. A typical system includes:

- A telephone interface unit
- The radio paging terminal
- A radio transmitter installation (base station)
- Up to 100 pocket-size paging receivers (tone-only or tone-and-voice)

Figure 1 depicts a typical configuration.

Selective radio paging is accomplished by transmitting an rf carrier which is frequency modulated by a series of audio tones, and in some cases by a voice message. Each paging recipient carries a pocket receiver that responds to a particular sequence of the audio tones. The receiver remains muted until the proper tones are received, after which an audible alert tone is produced. In the case of a tone-only page, this alert tone is a signal for the paged person to perform some prearranged action, such as calling a telephone number or reporting to a specific location. For a tone-and-voice page, the alerting tone is followed by a voice message of variable length.

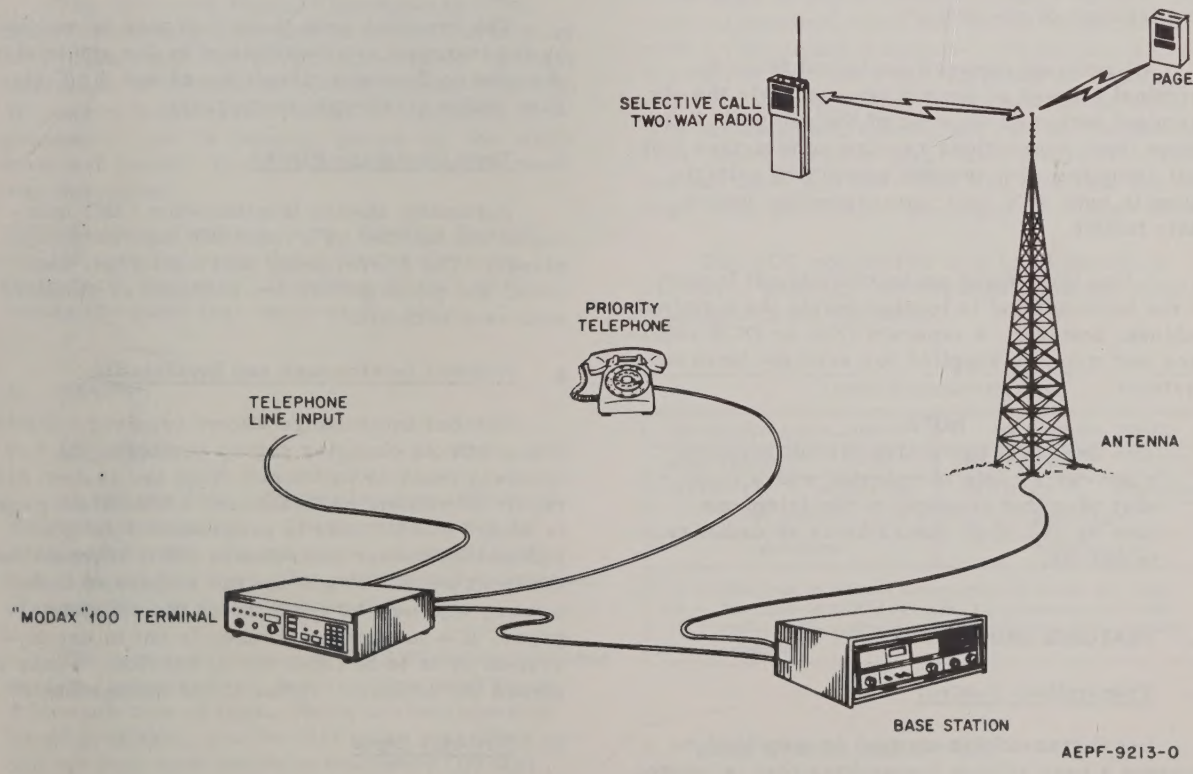


Figure 1. Typical System Configuration

2. PHYSICAL DESCRIPTION

The basic terminal is housed in a self-contained cabinet. It can be operated as a stand-alone desk-top unit, or it can be mounted within an existing 19-inch or 23-inch rack with suitable hardware provided. For flat surface mounting, rubber feet are provided.

Both discrete components and integrated circuitry are used throughout the system. All paging circuits are assembled on plug-connected printed circuit boards constructed of epoxy glass fiber. Several circuits are generally included on each circuit board so that only five boards are required. An integral power supply assembly and a tape cartridge player, for automatic station identification (ASI) messages, are provided. A status panel is also included which provides indicator lamps and a test telephone input jack for system maintenance.

The terminal is factory-wired for 115 V ac/13.8 V dc operation, with a maximum current requirement of one ampere.

All external connections to and from the terminal (except ac power) are made via the six terminal strips at the rear of the cabinet. Telephone input connections require an interface unit that complies with network protection criteria given in both FCC and corresponding intrastate tariffs.

A line level input protective circuit is part of the terminal and is located inside the terminal cabinet, however, a separate DCK or DCW interface unit must be supplied for selector level input systems.

NOTE

The line level protective circuit includes a two-wire cable terminated with a modular plug that connects to the telephone line tip and ring, the same as an ordinary telephone.

3. FEATURES AND OPTIONS

a. Transmitter Control

Local transmitter control is provided to operate a base station transmitter that is located close enough to the terminal such that a telephone line is not needed to interconnect the units. This usually means that the distance between the terminal and transmitter is limited to approximately 50 feet. For greater distances, the transmitter should be operated via a remote control console located near the terminal.

b. Shared-Channel (Monitor) Operation

For shared-channel operation, the terminal institutes a "monitor" cycle which checks for the presence of audio from the co-channel user. During the monitor time, reverse-channel audio is fed back from the base station to the caller.

c. Call Allotment Time

The amount of time allotted to each call can be changed from a standard 13 seconds to any period from 0 to 30 seconds by changing a timing resistor.

d. Lockout Control

If two terminals are sharing the same transmitter, lockout provisions are included to prevent one terminal from interfering with the other. Relay contact closures are provided for this purpose.

e. Code Plan Selection

The two-tone code types that may be encoded by the terminal are determined by the synthesizer circuits on the main circuit board and the Code Plan ROMs (read-only memories).

f. Tape Cartridge Player

Automatic station identification (ASI) messages are handled by a magnetic tape cartridge player. The prerecorded tape cartridge, tape deck, and preamplifier are included as standard with each terminal.

g. Number Interchange and Invalidation

Number interchange allows receiver substitution without changing paging numbers. If a receiver must be withdrawn from the system for repair or routine maintenance, a substitute pager is issued and its code is programmed via the Universal Number Interchange (UNI) keyboard on the front panel. Pages for the withdrawn code number will now be received on the substitute pager. If a subscriber number is not in use in a system or is to be taken out of service, it may be placed on "inactive" status in the same manner.

h. Priority Input

An optional priority telephone can be used with either a rotary dial or tone input. The priority telephone connects to the rear of the terminal, and when taken off-hook, will override any page currently in process, locking-out any other input (except the emergency page option, if so equipped).

i. Subaudible Paging

This optional feature provides the ability to handle simultaneous transmission of paging calls and two-way mobile communications using the same transmitter. Low frequency paging tones at low carrier deviations are used so that very little audible response will be produced in co-channel receivers engaged in audio communications. Subaudible paging also requires that the transmitter be equipped with a "Private-Line" kit, and the mobile system must be equipped for carrier squelch.

j. Two-Way Operation

The Model E09DAL0100AC Terminal is identical to the E09DAL0100AP Model, except that an additional circuit board is included to accommodate two-way communications between the Sending Party* and the Receiving Party*. To accomplish this, the Receiving Party must be equipped with a compatible "Selective-Call" two-way portable radio.

The Universal Number Interchange (UNI) allows individual receivers in a mixed system to be programmed for either one-way or two-way operation. If the UNI is deleted (Option R080AA), all pagers in the system must be internally programmed, via a jumper option on the main terminal board, for exclusive one-way or two-way operation.

*NOTE: Henceforth the term "Sending Party" shall denote the party that initiates the page. Henceforth the term "Receiving Party" shall denote the party that receives the page.

4. INPUTS

a. General

There are four different input boards available for the terminal. The terminal must be ordered with the correct board, depending upon how it is used in the paging system and the method of connecting to the telephone line.

The terminal is used in a PABX interconnected system (selector level input or line level input). With each type of input, there are two types of board available, one for dial pulse signalling and one for dual-tone multiple-frequency (DTMF) tone signalling.

b. Selector Level Inputs

In a PABX-interconnected system, the ordinary dial-pulse or tone-coded telephones of a telephone exchange become the dispatch points, and a page can be originated from any telephone in the system.

In selector-level systems, the telephone company equipment automatically routes all calls to the terminal, whenever a pre-determined single-digit paging prefix number is dialed. As soon as the terminal is accessed, a go-ahead tone (short duration beep) will be returned and the caller can then dial the two-digit code number for the pager he wishes to reach.

The selector level input requires a telephone-company-supplied external interface circuit (DCK/DCW) between the terminal and the exchange.

c. Line Level Inputs

In an end-to-end system, the terminal is connected to the telephone line tip and ring, the same as an ordinary telephone. Any caller with a knowledge of the terminal telephone number can call the terminal via a dial-pulse telephone or with a tone-coded telephone. To initiate a page, the caller first dials the telephone or extension number, as applicable, to access the terminal. The terminal will answer the call with a go-ahead tone (short duration beep) after a three- or four-second delay and the caller can then dial the two-digit code number for the pager he wishes to reach.

The FCC registered line-level interface circuit is built into the terminal, and the RDMZR interface is not required.

INPUT BOARD APPLICATIONS			
SELECTOR LEVEL INPUT		LINE LEVEL INPUT	
DIAL PULSE	TONE	DIAL PULSE*	TONE
NLN5111A	NLN5113A	NLN5110A	NLN5112A
TELEPHONE LINE INTERFACE REQUIRED			
DCK/DCW		NLN1466A**	

* = This type of input is not operational at all locations.
** = The built-in NLN5114A Line Level Interface Circuit replaces the external RDMZR interface unit normally required.

5. BASIC SYSTEM DESCRIPTION

The "MODAX" 100 Terminal is normally supplied with a selector level dial pulse input board, universal number interchange, main terminal board without emergency page, and an automatic station identifier assembly. Figure 2 is a simplified block diagram showing the basic

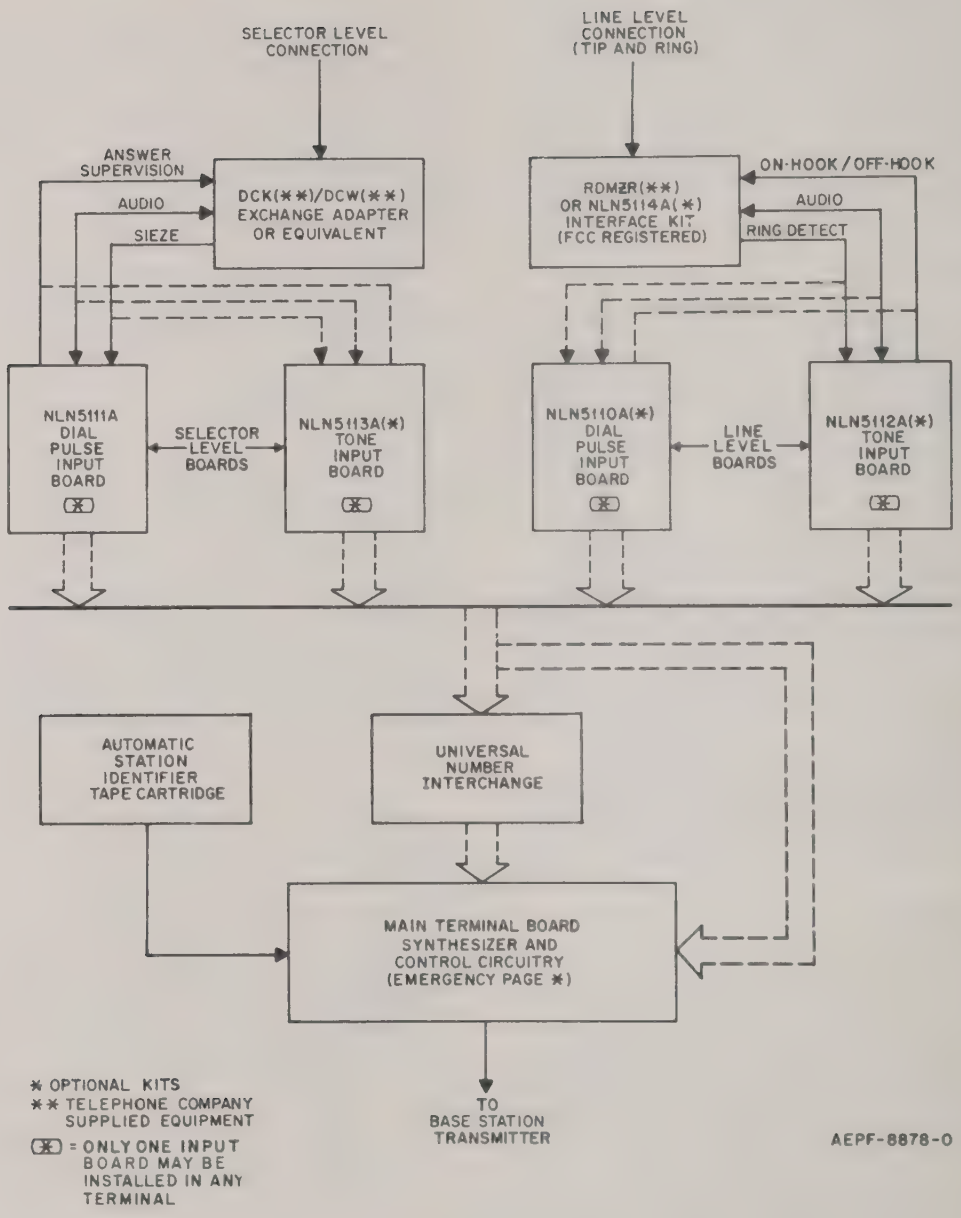

SELECTOR LEVEL CONNECTION
LINE LEVEL CONNECTION (TIP AND RING)
ANSWER SUPERVISION
AUDIO
SIEZE
DCK(**)/DCW(**) EXCHANGE ADAPTER OR EQUIVALENT
RDMZR(**) OR NLN5114A(*) INTERFACE KIT (FCC REGISTERED)
ON-HOOK / OFF-HOOK
AUDIO
RING DETECT
NLN5111A DIAL PULSE INPUT BOARD
SELECTOR LEVEL BOARDS
NLN5113A(*) TONE INPUT BOARD
NLN5110A(*) DIAL PULSE INPUT BOARD
LINE LEVEL BOARDS
NLN5112A(*) TONE INPUT BOARD
AUTOMATIC STATION IDENTIFIER TAPE CARTRIDGE
UNIVERSAL NUMBER INTERCHANGE
MAIN TERMINAL BOARD SYNTHESIZER AND CONTROL CIRCUITRY (EMERGENCY PAGE *)
TO BASE STATION TRANSMITTER
* OPTIONAL KITS
** TELEPHONE COMPANY SUPPLIED EQUIPMENT
= ONLY ONE INPUT BOARD MAY BE INSTALLED IN ANY TERMINAL
AEPF-8878-0

Figure 2. Simplified Terminal Block Diagram

system with the telephone company or Motorola interfaces required for the alternate input board options, if selected. The following paragraphs describe a standard system with no options installed. The optional input board and interface requirements are covered in detail in the theory of operation section of this manual.

To initiate a page, the caller first dials the single-digit access code for the terminal. If the system is on and "in service," it presents the interface unit with a contact closure that indicates this condition and thereby enables operation to take place. If the input is not busy, a second contact closure is presented to the interface unit, and a "go-ahead" tone (short duration pulse) is returned to the caller. This indicates that the terminal is ready and the pager code may be dialed.

If the terminal is not "in-service" or if a page is in process, a busy signal is returned to the caller and he must hand up and re-dial the access code. A continual ringback from the terminal indicates a "lockout" condition, where the universal number interchange is in use or the base station is transmitting a page from a co-channel user. This is a temporary condition and the caller may either stay on the line until the terminal is free (indicated by a "go-ahead" tone) or hang up and try later.

When the two-digit pager code is dialed, a string of serial pulses is generated for each input digit and presented as contact closures to the input board. The input board responds by detecting and decoding the signals received from the interface unit. The resulting pager number is then processed.

The pager digits are sent to the main terminal board via the universal number interchange, where the number is checked for valid/invalid status. When an inactive number is dialed, a warbling alarm is returned to the caller, indicating that the paging call cannot be transmitted for that number. When a pager is taken out of service for maintenance and the subscriber is assigned a replacement with a different pager code, the universal number interchange is programmed to automatically substitute the replacement pager code for the dialed number.

When the pager number is being processed by the terminal, an "acknowledgment" (beeping) signal is returned to the user and when this signal stops, the caller may proceed with his voice message.

Included in the cabinet is an automatic station identification (ASI) control circuit which periodically starts a magnetic tape cartridge player. The prerecorded tape ASI message is transmitted automatically at approximately 26 minutes following the first paging call of a paging sequence. If no paging calls are made since the last ASI message, the tape player is not activated.

The main terminal circuit board includes the synthesizer, timing, and control circuitry required to convert the paging numbers into the proper audio paging tones with the correct timing for two-tone paging operation. This is accomplished by using a programmable counter to divide a master clock frequency down to the desired frequency range. Read-only memories (ROMs) are used to convert numbers into counter preset values. A digital-to-analog converter then generates an output sinewave signal which, after filtering, is suitable for application to the base station transmitter.

6. SPECIAL TERMS AND ABBREVIATIONS

Some servicemen may not be familiar with the terminology used in paging terminals manufactured by Motorola, or with the special abbreviations used by the industry. Appendix A in the back of this manual is a glossary of terms and abbreviations used to describe the terminal and the telephone equipment used to interface the paging terminal to the telephone system.

TONE CODING

1. INTRODUCTION

Motorola radio paging systems employing the "MODAX" 100 Terminal use two-tone sequential signaling (refer to Figure 1). Two discrete audio tones (tone A and tone B) are transmitted for a specific period of time. Each pager in the system responds to a unique combination of tones, which is determined by filters installed in the pager. The types of paging calls that may be generated by the paging system are determined by the coding type circuits and the programming of tones into the tone synthesizer circuitry of the paging terminal. These functions are implemented mainly by special read-only memories (ROMs) which are programmed according to a desired code plan or code type for the paging terminal.

2. CODE PLAN DESCRIPTION

There are a number of different code plans used in paging systems. Each code plan has a letter designator that defines the code plan and its associated tone groups (refer to Table 1). Each tone group contains ten frequencies (refer to Tables 2 through 21). Tables 2 through 21 show the correlation between tone group's tone number, pager units or tens digit, frequency, and ROM output bits. Through the use of Tables 1 through 21 and the pager code (cap code), the frequencies of the two audio selective elements used in the pager decoding circuit can be determined. In addition to the standard code plans listed in Table 1, groups 10 and 11 are available.

a. Paging Code Plans

The code plans used in the paging system are shown in Table 1. The code plan letter designator is listed in the left-hand column of the table (B through GE). The numbers listed to the right of the code plan designator indicate the tone groups available for that code plan. These paging terminals are programmed for one tone group out of a code plan. For example, a paging terminal using code plan C will be programmed for either tone group 1, 2, or 4; for code plan AZ, a paging terminal will be programmed for either tone group 17, 18, or 19. Code plan Y is used for "Quik-Call" systems. Code plans AZ and 8AZ are used for subaudible systems. Code plan GE is used for General Electric Co. paging systems.

Table 1.
Code Plan Designator and Tone Group Used

CODE PLAN DESIGNATOR	TONE GROUP USED		
B	1	2	3
C	1	2	4
D	1	2	5
E	1	2	6
F	1	3	4
G	1	3	5
H	1	3	6
J	1	4	5
K	1	4	6
L	1	5	6
M	2	3	4
N	2	3	5
P	2	3	6
Q	2	4	5
R	2	4	6
S	2	5	6
T	3	4	5
U	3	4	6
V	3	5	6
W	4	5	6
Y	A(QC)	B(QC)	Z(QC)
AZ	17	18	19
8AZ	17x8	18x8	19x8
GE	A(GE)	B(GE)	C(GE)

In paging systems, a call code consists of a letter prefix and a three-digit number. The letter prefix designates the code plan or code type. The most significant digit is used to determine from which tone group that the first and second tone burst tones are selected. For example, assume a system operating in code plan D which indicates that tone groups 1, 2, or 5 are used (shown in Table 1). Next, assume that the pager to be paged has a cap code of D214. The most significant digit is 2 which means that the first tone and the second tone will be a tone from tone group 2. The second and third digits of the call code determine the tone number selected from the tone group. The second digit, number 1, indicates the first tone to be tone number 1 of tone group 2 (600.9 Hz). See Table 3. The third digit, number 4, indicates the second tone to be tone number 4 of tone group 2 (707.3 Hz).

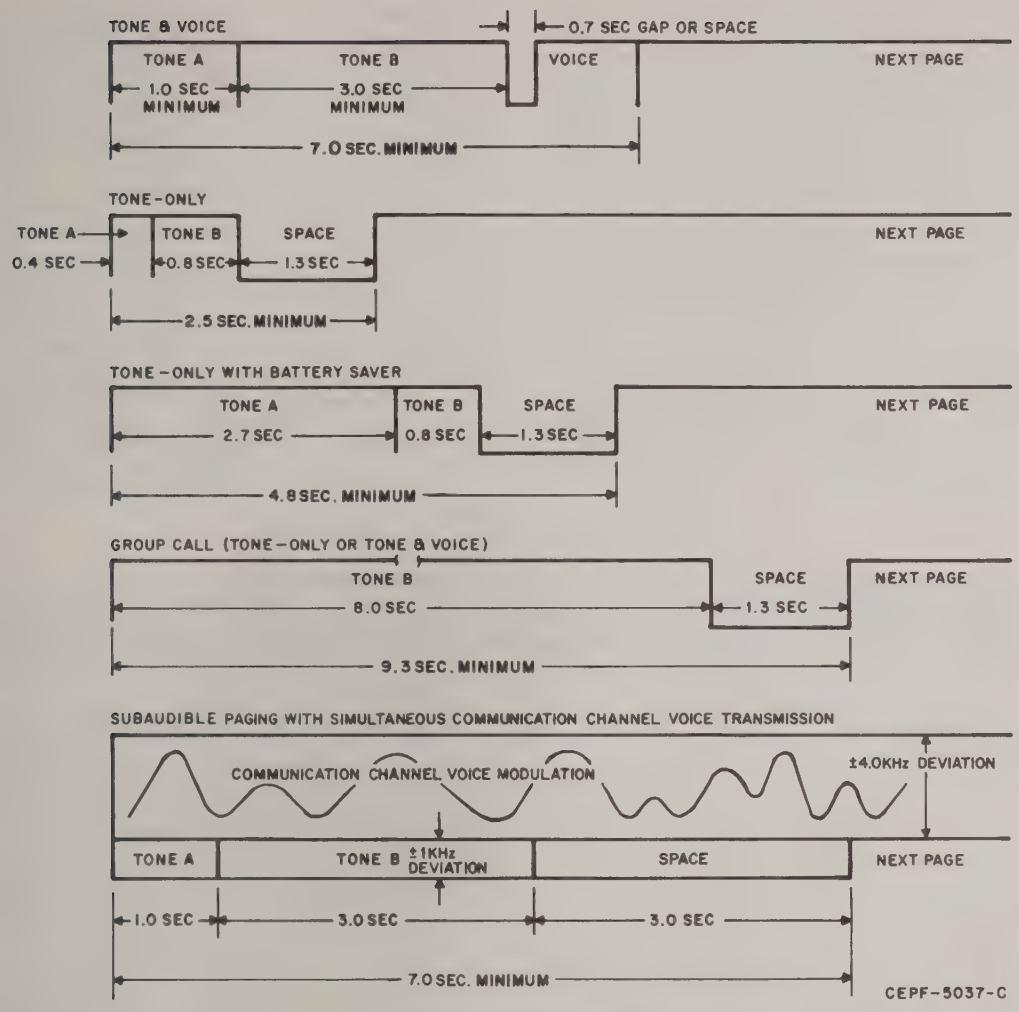
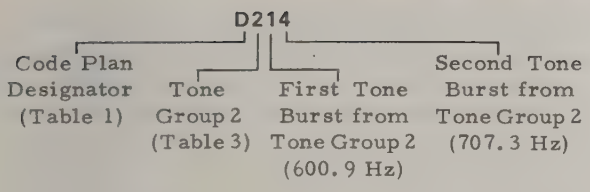


Figure 3. Two-Tone Signalling Options


D214
Code Plan Designator (Table 1)
Tone Group 2 (Table 3)
First Tone Burst from Tone Group 2 (600.9 Hz)
Second Tone Burst from Tone Group 2 (707.3 Hz)

Refer to any one of Tables 2 through 21; notice the correlation between the tone number column and the pager digits. For the preceding example (D214), pager number 14 is dialed to page pager code D214.

b. Subaudible Tone Coding

Subaudible coding provides the facility for simultaneous transmission of paging calls and voice communications on the same channel. Low frequency paging tones from 67.0 to 202.7 Hz at a low carrier deviation of 0.5 to 1 kHz are used so that no audible response will be produced in co-channel receivers engaged in audio communications.

Subaudible paging codes differ from the standard paging codes due to the low frequency required. The subaudible tone groups are designated groups 17, 18, 19, 17x8, 18x8, and 19x8 in Tables 10 through 15. Determination of frequencies is identical to that described in the preceding paragraph.

c. Group Call Coding

Pagers with the group call option are assigned two code numbers: one for individual call and one for group call. If the individual number is used to call a group pager, it alone will be alerted as is the standard pager. If the group call number is used, all other pagers in the same group will be alerted along with this pager.

Group call is accomplished by transmitting a single continuous tone for approximately eight seconds. This tone will alert all group call pagers that use this tone frequency in the tone B position.

An example of a pager code with group call is as follows: D567/177, where 177 is the group call number. The first digit gives the tone group and the second and third digits correspond to the tone number; therefore, 177 means tone number 7 from tone group 1. According to Table 2, the group call tone for this pager is 483.5 Hz.

The maximum number of pagers that may be included in a group is equal to the total number of paging tones available in the paging encoder, minus one. The maximum number of groups in a system is equal to the number of paging tones available.

d. Tone Timing

The different timings associated with various two-tone signalling options are shown in Figure 1. To implement these different timings, resistor values are changed at certain parts of the paging encoder circuitry, which is explained in the "Setup Procedures" section of this manual.

Table 2. Tone Group 1 Frequencies and ROM Outputs

TONE NUMBER	PAGER NO.		FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS															
	TENS DIGIT	UNITS DIGIT		2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	330.5	0	0	1	1	0	0	1	1	0	0	0	0	0	1	0	1
1	1	1	349.0	0	0	1	1	0	1	0	0	1	0	0	1	0	0	0	0
2	2	2	368.5	0	0	1	1	0	1	1	0	1	0	0	0	0	1	0	1
3	3	3	389.0	0	0	1	1	1	0	0	0	1	0	0	1	0	0	0	0
4	4	4	410.8	0	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0
5	5	5	433.7	0	1	0	0	0	0	1	1	0	0	1	1	0	1	1	1
6	6	6	457.9	0	1	0	0	0	1	0	1	0	1	1	1	1	0	0	1
7	7	7	483.5	0	1	0	0	1	0	0	0	0	0	1	1	0	1	0	1
8	8	8	510.5	0	1	0	1	0	0	0	1	0	0	0	0	0	1	0	1
9	9	9	539.0	0	1	0	1	0	0	1	1	1	0	0	1	0	0	0	0

Table 3. Tone Group 2 Frequencies and ROM Outputs

TONE NUMBER	PAGER NO.		FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS															
	TENS DIGIT	UNITS DIGIT		2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	569.1	0	1	0	1	0	1	1	0	1	0	0	1	0	0	0	1
1	1	1	600.9	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	1
2	2	2	634.5	0	1	1	0	0	0	1	1	0	1	0	0	0	1	0	1
3	3	3	669.9	0	1	1	0	0	1	1	0	1	0	0	1	1	0	0	1
4	4	4	707.3	0	1	1	1	0	0	0	0	0	1	1	1	0	0	1	1
5	5	5	746.8	0	1	1	1	0	1	0	0	0	1	1	0	1	0	0	0
6	6	6	788.5	0	1	1	1	1	0	0	0	1	0	0	0	0	1	0	1
7	7	7	832.5	1	0	0	0	0	0	1	1	0	0	1	0	0	1	0	1
8	8	8	879.0	1	0	0	0	0	1	1	1	1	0	0	1	0	0	0	0
9	9	9	928.1	1	0	0	1	0	0	1	0	1	0	0	0	0	0	0	1

Table 4. Tone Group 3 Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	1092.4	1	1	0	1	0	0	0	0	1	0	0	1	0	0	1	0
1	1	1	288.5	0	0	1	0	1	0	0	0	1	0	0	0	0	1	0	1
2	2	2	296.5	0	0	1	0	1	0	0	1	0	1	1	0	0	1	0	1
3	3	3	304.7	0	0	1	1	0	0	0	0	0	1	0	0	0	1	1	1
4	4	4	313.0	0	0	1	1	0	0	0	1	0	0	1	1	0	0	0	0
5	5	5	953.7	1	0	0	1	0	1	0	1	0	0	1	1	0	1	1	1
6	6	6	979.9	1	0	0	1	0	1	1	1	1	0	0	1	1	0	0	1
7	7	7	1006.9	1	1	0	1	0	0	0	0	0	0	0	0	0	1	1	0
8	8	8	1034.7	1	1	0	1	0	0	0	0	0	0	1	1	0	1	0	0
9	9	9	1063.2	1	1	0	1	0	0	0	0	0	1	1	0	0	1	0	0

Table 5. Tone Group 4 Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	321.7	0	0	1	1	0	0	1	0	0	0	0	1	0	1	1	1
1	1	1	339.6	0	0	1	1	0	0	1	1	1	0	0	1	0	1	1	0
2	2	2	358.6	0	0	1	1	0	1	0	1	1	0	0	0	0	1	1	0
3	3	3	378.6	0	0	1	1	0	1	1	1	1	0	0	0	0	1	1	0
4	4	4	399.8	0	0	1	1	1	0	0	1	1	0	0	1	1	0	0	0
5	5	5	422.1	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0	1
6	6	6	445.7	0	1	0	0	0	1	0	0	0	1	0	1	0	1	1	1
7	7	7	470.5	0	1	0	0	0	1	1	1	0	0	0	0	0	1	0	1
8	8	8	496.8	0	1	0	0	1	0	0	1	0	1	1	0	1	0	0	0
9	9	9	524.6	0	1	0	1	0	0	1	0	0	1	0	0	0	1	1	0

Table 6. Tone Group 5 Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	553.9	0	1	0	1	0	1	0	1	0	0	1	1	1	0	0	1
1	1	1	584.8	0	1	0	1	1	0	0	0	0	1	0	0	1	0	0	0
2	2	2	617.4	0	1	1	0	0	0	0	1	0	1	1	1	0	1	0	0
3	3	3	651.9	0	1	1	0	0	1	0	1	0	0	0	1	1	0	0	1
4	4	4	688.3	0	1	1	0	1	0	0	0	1	0	0	0	0	0	1	1
5	5	5	726.8	0	1	1	1	0	0	1	0	0	1	1	0	1	0	0	0
6	6	6	767.4	0	1	1	1	0	1	1	0	0	1	1	1	0	1	0	0
7	7	7	810.2	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0
8	8	8	855.5	1	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1
9	9	9	903.2	1	0	0	1	0	0	0	0	0	0	1	1	0	0	1	0

Table 7. Tone Group 6 Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	1122.5	1	1	0	1	0	0	0	1	0	0	1	0	0	0	1	0
1	1	1	1153.4	1	1	0	1	0	0	0	1	0	1	0	1	0	1	0	0
2	2	2	1185.2	1	1	0	1	0	0	0	1	1	0	0	0	0	1	1	0
3	3	3	1217.8	1	1	0	1	0	0	1	0	0	0	0	1	1	0	0	0
4	4	4	1251.4	1	1	0	1	0	0	1	0	0	1	0	1	0	0	1	0
5	5	5	1285.8	1	1	0	1	0	0	1	0	1	0	0	0	0	1	1	0
6	6	6	1321.2	1	1	0	1	0	0	1	1	0	0	1	0	0	0	1	0
7	7	7	1357.6	1	1	0	1	0	0	1	1	0	1	0	1	1	0	0	0
8	8	8	1395.0	1	1	0	1	0	0	1	1	1	0	0	1	0	1	1	0
9	9	9	1433.4	1	1	0	1	0	1	0	0	0	0	1	1	0	1	0	0

Table 8. Tone Group 10 Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	1472.9	1	1	0	1	0	1	0	0	0	1	1	1	0	0	1	0
1	1	1	1513.5	1	1	0	1	0	1	0	1	0	0	0	1	0	1	0	0
2	2	2	1555.2	1	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0
3	3	3	1598.0	1	1	0	1	0	1	0	1	1	0	0	1	1	0	0	0
4	4	4	1642.0	1	1	0	1	0	1	1	0	0	1	0	0	0	0	1	0
5	5	5	1687.2	1	1	0	1	0	1	1	0	1	0	0	0	1	0	0	0
6	6	6	1733.7	1	1	0	1	0	1	1	1	0	0	1	1	0	1	0	0
7	7	7	1781.5	1	1	0	1	0	1	1	1	1	0	0	0	0	0	1	0
8	8	8	1830.5	1	1	0	1	1	0	0	0	0	0	1	1	0	0	0	0
9	9	9	1881.0	1	1	0	1	1	0	0	0	1	0	0	0	0	0	1	0

Table 9. Tone Group 11 Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	1930.2	1	1	0	1	1	0	0	1	0	0	1	1	0	0	0	0
1	1	1	1989.0	1	1	0	1	1	0	0	1	1	0	0	1	0	0	0	0
2	2	2	2043.8	1	1	1	0	0	0	0	0	0	1	0	0	0	1	0	0
3	3	3	2094.5	1	1	1	0	0	0	0	0	1	0	0	1	0	1	0	0
4	4	4	2155.6	1	1	1	0	0	0	0	1	0	1	0	1	0	1	1	0
5	5	5	2212.2	1	1	1	0	0	0	1	0	0	0	0	1	0	0	1	0
6	6	6	2271.7	1	1	1	0	0	0	1	0	0	1	1	1	0	0	1	0
7	7	7	2334.6	1	1	1	0	0	0	1	1	0	0	1	1	0	1	0	0
8	8	8	2401.0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	1	0
9	9	9	2468.2	1	1	1	0	0	1	0	0	0	1	1	0	1	0	0	0

Table 10. Tone Group 17 Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	146.2	0	0	0	1	0	1	0	0	0	1	1	0	0	0	1	0
1	1	1	202.7	0	0	1	0	0	0	0	0	0	0	1	0	0	1	1	1
2	2	2	192.8	0	0	0	1	1	0	0	1	0	0	1	0	1	0	0	0
3	3	3	186.2	0	0	0	1	1	0	0	0	0	1	1	0	0	0	1	0
4	4	4	69.3	0	0	0	0	0	1	1	0	1	0	0	1	0	0	1	1
5	5	5	173.8	0	0	0	1	0	1	1	1	0	0	1	1	1	0	0	0
6	6	6	167.9	0	0	0	1	0	1	1	0	0	1	1	1	1	0	0	1
7	7	7	162.2	0	0	0	1	0	1	1	0	0	0	1	0	0	0	1	0
8	8	8	156.7	0	0	0	1	0	1	0	1	0	1	1	0	0	1	1	1
9	9	9	151.4	0	0	0	1	0	1	0	1	0	0	0	1	0	1	0	0

Table 11. Tone Group 18 Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	103.5	0	0	0	1	0	0	0	0	0	0	1	1	0	1	0	1
1	1	1	141.3	0	0	0	1	0	1	0	0	0	0	0	1	0	0	1	1
2	2	2	136.5	0	0	0	1	0	0	1	1	0	1	1	0	0	1	0	1
3	3	3	131.8	0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	0
4	4	4	127.3	0	0	0	1	0	0	1	0	0	1	1	1	0	0	1	1
5	5	5	123.0	0	0	0	1	0	0	1	0	0	0	1	1	0	0	0	0
6	6	6	74.4	0	0	0	0	0	1	1	1	0	1	0	0	0	1	0	0
7	7	7	114.8	0	0	0	1	0	0	0	1	0	1	0	0	1	0	0	0
8	8	8	110.9	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	1
9	9	9	107.2	0	0	0	1	0	0	0	0	0	1	1	1	0	0	1	0

Table 12. Tone Group 19 Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	67.0	0	0	0	0	0	1	1	0	0	1	1	1	0	0	0	0
1	1	1	100.0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
2	2	2	79.7	0	0	0	0	0	1	1	1	1	0	0	1	0	1	1	1
3	3	3	94.8	0	0	0	0	1	0	0	1	0	1	0	0	1	0	0	0
4	4	4	91.5	0	0	0	0	1	0	0	1	0	0	0	1	0	1	0	1
5	5	5	88.5	0	0	0	0	1	0	0	0	1	0	0	0	0	1	0	1
6	6	6	85.4	0	0	0	0	1	0	0	0	0	1	0	1	0	1	0	0
7	7	7	82.5	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	1
8	8	8	77.0	0	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0
9	9	9	71.9	0	0	0	0	0	1	1	1	0	0	0	1	1	0	0	1

Table 13. Tone Group 17 x (8) Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	1169.6	1	1	0	1	0	0	0	1	0	1	1	1	0	0	0	0
1	1	1	1621.6	1	1	0	1	0	0	1	0	0	0	1	0	0	0	1	0
2	2	2	1542.4	1	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0
3	3	3	1489.6	1	1	0	1	0	1	0	0	1	0	0	1	0	0	0	0
4	4	4	554.4	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0
5	5	5	1390.4	1	1	0	1	0	0	1	1	1	0	0	1	0	0	0	0
6	6	6	1343.2	1	1	0	1	0	0	1	1	0	1	0	0	0	1	0	0
7	7	7	1297.6	1	1	0	1	0	0	1	0	1	0	0	1	1	0	0	0
8	8	8	1253.6	1	1	0	1	0	0	1	0	0	1	0	1	0	1	0	0
9	9	9	1211.2	1	1	0	1	0	0	1	0	0	0	0	1	0	0	1	0

Table 14. Tone Group 18 x (8) Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	828.0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0
1	1	1	1130.4	1	1	0	1	0	0	0	1	0	0	1	1	0	0	0	0
2	2	2	1092.0	1	1	0	1	0	0	0	0	1	0	0	1	0	0	1	0
3	3	3	1054.4	1	1	0	1	0	0	0	0	0	1	0	1	0	1	0	0
4	4	4	1018.4	1	1	0	1	0	0	0	0	0	0	0	1	1	0	0	0
5	5	5	984.0	1	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0
6	6	6	595.7	0	1	0	1	1	0	0	1	0	1	0	1	0	1	1	1
7	7	7	918.4	1	0	0	1	0	0	0	1	1	0	0	0	0	1	0	0
8	8	8	887.2	1	0	0	0	1	0	0	0	0	1	1	1	0	0	1	0
9	9	9	857.6	1	0	0	0	0	1	0	1	0	1	1	1	0	1	1	0

Table 15. Tone Group 19 x (8) Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	536.0	0	1	0	1	0	0	1	1	0	1	1	0	0	0	0	0
1	1	1	800.0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	2	2	637.6	0	1	1	0	0	0	1	1	0	1	1	1	0	1	1	0
3	3	3	758.4	0	1	1	1	0	1	0	1	1	0	0	0	0	1	0	0
4	4	4	732.0	0	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0
5	5	5	708.0	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0
6	6	6	683.2	0	1	1	0	1	0	0	0	0	0	1	1	0	0	1	0
7	7	7	660.0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0
8	8	8	616.0	0	1	1	0	0	0	0	1	0	1	1	0	0	0	0	0
9	9	9	575.2	0	1	0	1	0	1	1	1	0	1	0	1	0	0	1	0

Table 16. Tone Group A (QC) Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	358.9	0	0	1	1	0	1	0	1	1	0	0	0	1	0	0	1
1	1	1	398.1	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	1
2	2	2	441.6	0	1	0	0	0	1	0	0	0	0	0	1	0	1	1	0
3	3	3	489.8	0	1	0	0	1	0	0	0	1	0	0	1	1	0	0	0
4	4	4	543.3	0	1	0	1	0	1	0	0	0	0	1	1	0	0	1	1
5	5	5	602.6	0	1	1	0	0	0	0	0	0	0	1	0	0	1	1	0
6	6	6	668.3	0	1	1	0	0	1	1	0	1	0	0	0	0	0	1	1
7	7	7	741.3	0	1	1	1	0	1	0	0	0	0	0	1	0	0	1	1
8	8	8	822.2	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0
9	9	9	912.0	1	0	0	1	0	0	0	1	0	0	1	0	0	0	0	0

Table 17. Tone Group B (QC) Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	371.5	0	0	1	1	0	1	1	1	0	0	0	1	0	1	0	1
1	1	1	412.1	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	1
2	2	2	457.1	0	1	0	0	0	1	0	1	0	1	1	1	0	0	0	1
3	3	3	507.0	0	1	0	1	0	0	0	0	0	1	1	1	0	0	0	0
4	4	4	562.3	0	1	0	1	0	1	1	0	0	0	1	0	0	0	1	1
5	5	5	623.7	0	1	1	0	0	0	1	0	0	0	1	1	0	1	1	1
6	6	6	691.8	0	1	1	0	1	0	0	1	0	0	0	1	1	0	0	0
7	7	7	767.4	0	1	1	1	0	1	1	0	0	1	1	1	0	1	0	0
8	8	8	851.1	1	0	0	0	0	1	0	1	0	0	0	1	0	0	0	1
9	9	9	944.1	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0	1

Table 18. Tone Group Z (QC) Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	346.7	0	0	1	1	0	1	0	0	0	1	1	0	0	1	1	1
1	1	1	384.6	0	0	1	1	1	0	0	0	0	1	0	0	0	1	1	0
2	2	2	426.6	0	1	0	0	0	0	1	0	0	1	1	0	0	1	1	0
3	3	3	473.2	0	1	0	0	0	1	1	1	0	0	1	1	0	0	1	0
4	4	4	524.8	0	1	0	1	0	0	1	0	0	1	0	0	1	0	0	0
5	5	5	582.1	0	1	0	1	1	0	0	0	0	0	1	0	0	0	0	1
6	6	6	645.7	0	1	1	0	0	1	0	0	0	1	0	1	0	1	1	1
7	7	7	716.1	0	1	1	1	0	0	0	1	0	1	1	0	0	0	0	1
8	8	8	794.3	0	1	1	1	1	0	0	1	0	1	0	0	0	0	1	1
9	9	9	881.0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Table 19. Tone Group A (GE) Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	682.5	0	1	1	0	1	0	0	0	0	0	1	0	0	1	0	1
1	1	1	592.5	0	1	0	1	1	0	0	1	0	0	1	0	0	1	0	1
2	2	2	757.5	0	1	1	1	0	1	0	1	0	1	1	1	0	1	0	1
3	3	3	802.5	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1
4	4	4	847.5	1	0	0	0	0	1	0	0	0	1	1	1	0	1	0	1
5	5	5	892.5	1	0	0	0	1	0	0	1	0	0	1	0	0	1	0	1
6	6	6	937.5	1	0	0	1	0	0	1	1	0	1	1	1	0	1	0	1
7	7	7	547.5	0	1	0	1	0	1	0	0	0	1	1	1	0	1	0	1
8	8	8	727.5	0	1	1	1	0	0	1	0	0	1	1	1	0	1	0	1
9	9	9	637.5	0	1	1	0	0	0	1	1	0	1	1	1	0	1	0	1

Table 20. Tone Group B (GE) Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	652.5	0	1	1	0	0	1	0	1	0	0	1	0	0	1	0	1
1	1	1	607.5	0	1	1	0	0	0	0	0	0	1	1	1	0	1	0	1
2	2	2	787.5	0	1	1	1	1	0	0	0	0	1	1	1	0	1	0	1
3	3	3	832.5	1	0	0	0	0	0	1	1	0	0	1	0	0	1	0	1
4	4	4	877.5	1	0	0	0	0	1	1	1	0	1	1	1	0	1	0	1
5	5	5	922.5	1	0	0	1	0	0	1	0	0	0	1	0	0	1	0	1
6	6	6	967.5	0	1	0	1	0	1	1	0	0	1	1	1	0	1	0	1
7	7	7	517.5	0	1	0	1	0	0	0	1	0	1	1	1	0	1	0	1
8	8	8	562.5	0	1	0	1	0	1	1	0	0	0	1	0	0	1	0	1
9	9	9	697.5	0	1	1	0	1	0	0	1	0	1	1	1	0	1	0	1

Table 21. Tone Group C (GE) Frequencies and ROM Outputs

TONE NUMBER	PAGER NO. TENS DIGIT	PAGER NO. UNITS DIGIT	FREQ (Hz)	READ-ONLY MEMORY OUTPUT BITS 2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
0	0	0	667.5	0	1	1	0	0	1	1	0	0	1	1	1	0	1	0	1
1	1	1	712.5	0	1	1	1	0	0	0	1	0	0	1	0	0	1	0	1
2	2	2	772.5	0	1	1	1	0	1	1	1	0	0	1	0	0	1	0	1
3	3	3	817.5	1	0	0	0	0	0	0	1	0	1	1	1	0	1	0	1
4	4	4	862.5	1	0	0	0	0	1	1	0	0	0	1	0	0	1	0	1
5	5	5	907.5	1	0	0	1	0	0	0	0	0	1	1	1	0	1	0	1
6	6	6	952.5	1	0	0	1	0	1	0	1	0	0	1	0	0	1	0	1
7	7	7	532.5	0	1	0	1	0	0	1	1	0	0	1	0	0	1	0	1
8	8	8	577.5	0	1	0	1	0	1	1	1	0	1	1	1	0	1	0	1
9	9	9	622.5	0	1	1	0	0	0	1	0	0	0	1	0	0	1	0	1

INSTALLATION

1. UNPACKING AND INSPECTION

a. General

As soon as possible after delivery, unpack the equipment and inspect it thoroughly. If any part of the equipment has been damaged in transit, report the extent of the damage to the transportation company immediately.

This unit has been inspected and adjusted to its recommended operating condition at the factory. Unless it has been handled roughly in transit or otherwise abused or tampered with, it should require only line input/output level adjustments which are described under PREOPERATIONAL ADJUSTMENTS.

b. Equipment Checks

Remove the two screws that secure the top cover. These screws are located toward the front panel, one on each side of the housing. Open the top cover, which is hinged at the rear, and verify the following:

(1) That all options (if applicable) are present and that all boards are securely mounted in their proper location.

(2) Check that there are no loose or broken wires.

(3) Check the mechanical operation of all pushbuttons to ensure that they operate without binding.

Close the top cover and replace the two screws.

2. GENERAL INSTALLATION REQUIREMENTS

To ensure optimum performance and reliability, adequate facilities should be available at the terminal location. Review the physical and electrical requirements outlined below before selecting a site for the installation.

a. Physical Requirements

Ambient temperature in the terminal room should be maintained between 32 and 120 degrees F. Relative humidity should remain between 45 and 95 percent. Under no circumstances should condensation be allowed.

The terminal should not be subjected to vibration or shock. Do not install the unit in rooms adjoining machine shops, printing presses, refrigeration equipment, or other similar types of high electrical noise and/or vibration environments. In some locations, filtering may be required to maintain a low dust area.

b. Electrical Requirements

(1) Power Connections

The terminal is factory-wired for 115 V ac ±10%, 60 Hz operation. Maximum current drawn by the system is one ampere. A power cord and plug are provided for connecting the unit to the power source.

For optimum performance, it is recommended that a three-wire power system, or an appropriate grounded plug adapter, be used.

NOTE

A terminal strip is provided on the rear panel for operation from a dc source during a power failure. Observe the polarity markings when connecting the battery.

(2) Interference

The performance of the terminal may be degraded by spurious signals received from outside sources. Minimize the possibility of interference by selecting a location away from generators of electrical noise such as large motors, switchgear, welding equipment, etc. The digital logic circuitry used in the terminal, although immune to most low-level interference, is particularly susceptible to discharges of static electricity. These discharges, which often reach high potentials, introduce errors and may cause erratic operation. Non-conductive household carpeting provides an excellent medium for the generation of static potentials and this type of floor covering is NOT recommended for use at the terminal site.

It is recommended that conductive carpeting or tile, manufactured especially for electronic installations, be used in the terminal room. If a conductive floor covering is not used, the area around the terminal should be sprayed with an anti-static compound. In periods of low humidity, this should be done at least once a

ek. A suitable chemical is supplied in spray s under the brand name "Static Stop," nufactured by Barco Chemical Products, cago, IL. Other equivalent products are ilable and these should serve just as well. vever, be sure that the product will not damage floor covering or the terminal housing.

MOUNTING

Flat Mounting

The terminal can be placed on any flat level face, such as a bench or desk top. Rubber are supplied for this type of mounting.

Rack Mounting

If it is desired to install the unit in an exist- cabinet or other equipment rack, use the N5119A mounting kit. The mounting brackets be used for either 19-inch or 23-inch rack unting by simply reversing the bracket orienta- , as required.

4. CONTROL POINT CONSIDERATIONS

FCC regulations require the ability to monitor and, if necessary, to terminate any inappropriate (illegal, obscene, etc,) transmissions or pages handled via the base station transmitter. To satisfy these requirements, a pushbutton disable switch and a speaker and volume control are located on the front panel of the terminal.

When the control operator is not in the immediate area of the terminal, some method of remote control must be implemented. A remote footswitch may be located at the base station or remote control console and connected to the L.O. (TB4-4) and COM (TB4-3) screws on the rear of the terminal to disable the "MODAX." Modifications to the base station or console may be required for monitoring. Figures 4 through 8 depict a variety of control point options that will satisfy the FCC requirements.

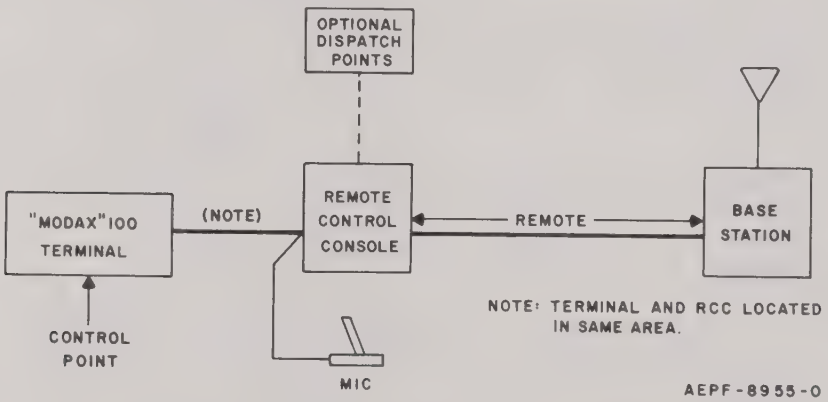


Figure 4. Terminal Designated Primary Control Point (Remote Operation)

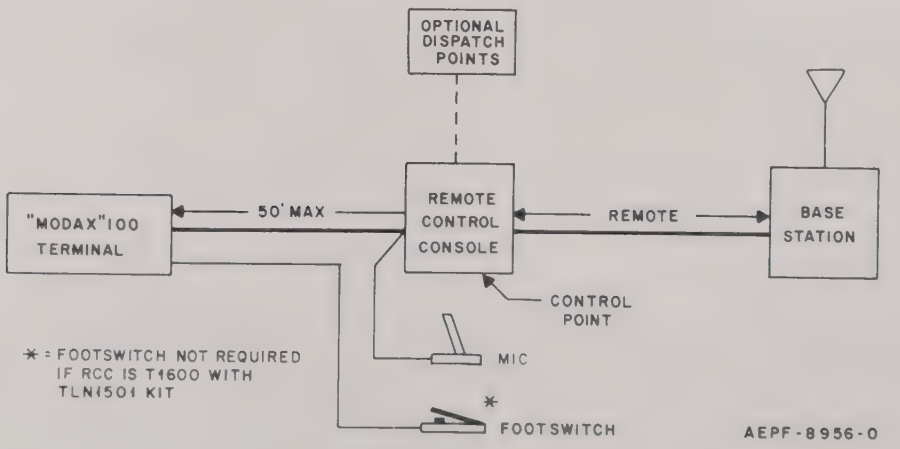


Figure 5. Local RCC Designated Primary Control Point (Remote Operation)

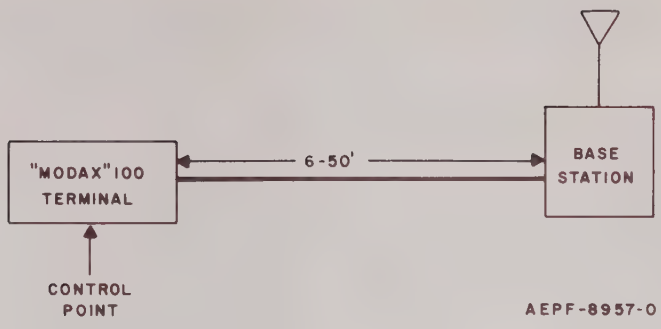


Figure 6. Terminal Designated Primary Control Point (Local Operation)

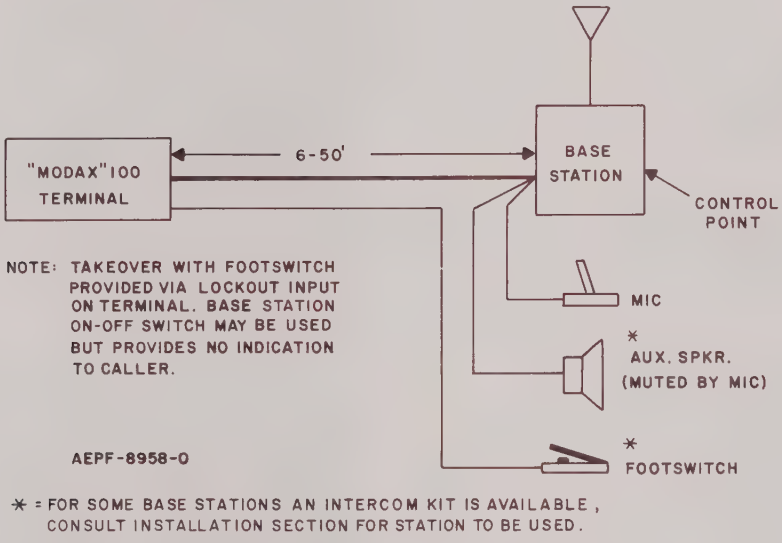

"MODAX" 100
TERMINAL
6-50'
BASE
STATION
CONTROL
POINT
NOTE: TAKEOVER WITH FOOTSWITCH PROVIDED VIA LOCKOUT INPUT ON TERMINAL. BASE STATION ON-OFF SWITCH MAY BE USED BUT PROVIDES NO INDICATION TO CALLER.
MIC
* AUX. SPKR. (MUTED BY MIC)
* FOOTSWITCH
AEPF-8958-0
* = FOR SOME BASE STATIONS AN INTERCOM KIT IS AVAILABLE, CONSULT INSTALLATION SECTION FOR STATION TO BE USED.

Figure 7. Base Station Designated Primary Control Point (Local Operation)

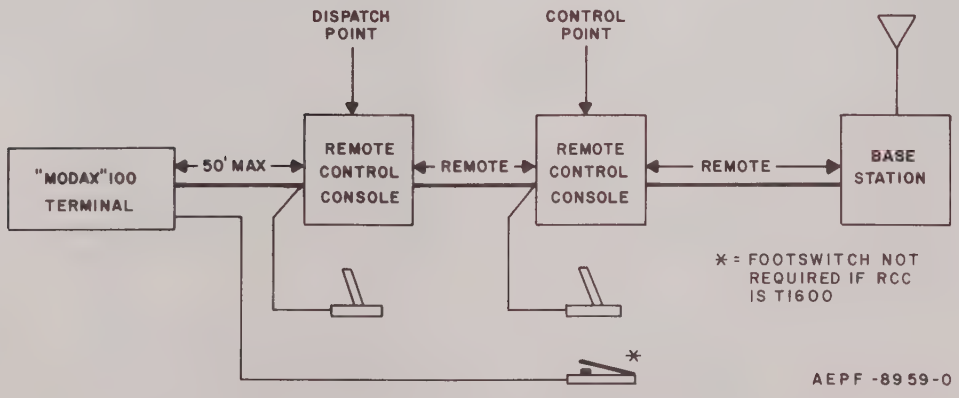


Figure 8. Remote RCC Designated Primary Control Point (Remote Operation)

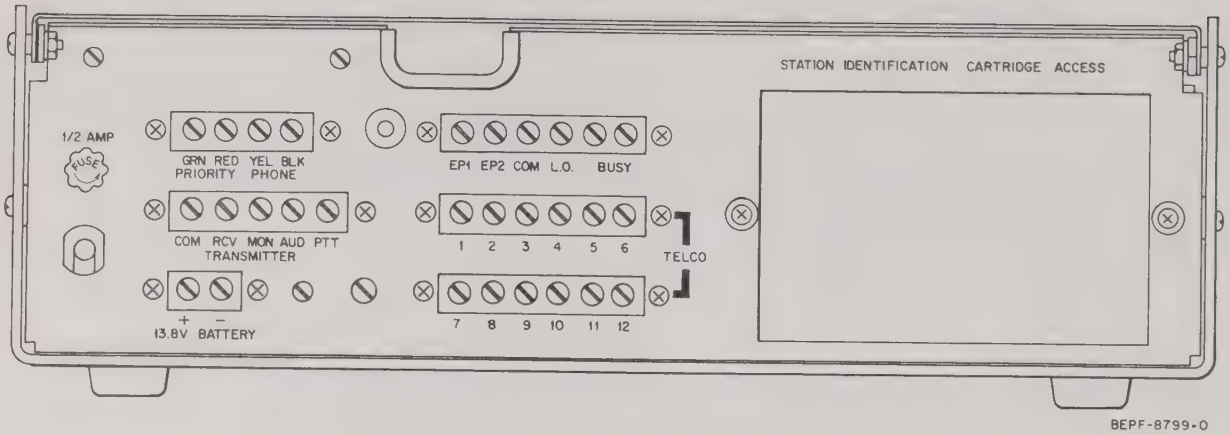


Figure 9. Rear View of "MODAX" 100 Terminal

5. EXTERNAL CONNECTIONS

a. General

All external connections to the terminal are made at the rear of the cabinet via six barrier type terminal strips (TB1 through TB6). The screw terminals are labeled as shown in Figure 9.

b. Priority Telephone Connections

When a priority telephone (NMN6075A/ NMN6076A) is included in the system, it is connected via TB1, a four-screw terminal strip labeled PRIORITY PHONE, as shown in Figure 10.

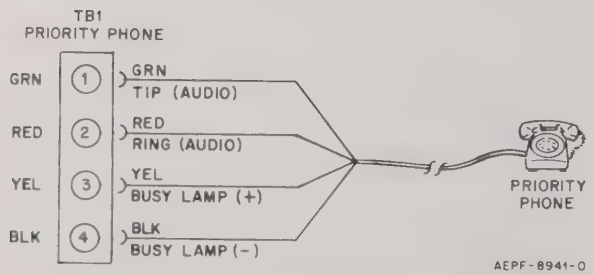


Figure 10. Priority Telephone Connections

The loop resistance presented to the RED and GRN terminals (including the priority phone) must be less than 1000 ohms with the priority phone off-hook. Also, the priority telephone must be located within the same facility as the terminal.

c. Base Station Connections

(1) Local Control

Connection of the terminal to a local control base station or remote control console for remote base station systems requires an accessory cable and in some cases modifications to the equipment. Figures 11 through 22 illustrate typical connections for the most common types of equipment. If your installation differs, refer to the instruction manual for your particular system. The following configurations are detailed in this section:

Figure 11. "Consolette" Base Station (PL)
Figure 12. "Consolette" Base Station (CS)
Figure 13. "Compa-Station" Base Station (PL)
Figure 14. "Compa-Station" Base Station (CS)
Figure 15. PT Series Base Station (CS)
Figure 16. "Maxar" Base Station
Figure 17. "Flexar" Base Station
Figure 18. T1200 Series Console
Figure 19. T1300 Series Console
Figure 20. T1450 Series Console
Figure 21. T1600 Series Console (DC & Tone)
Figure 22. T1600 Series Console (HEAR)

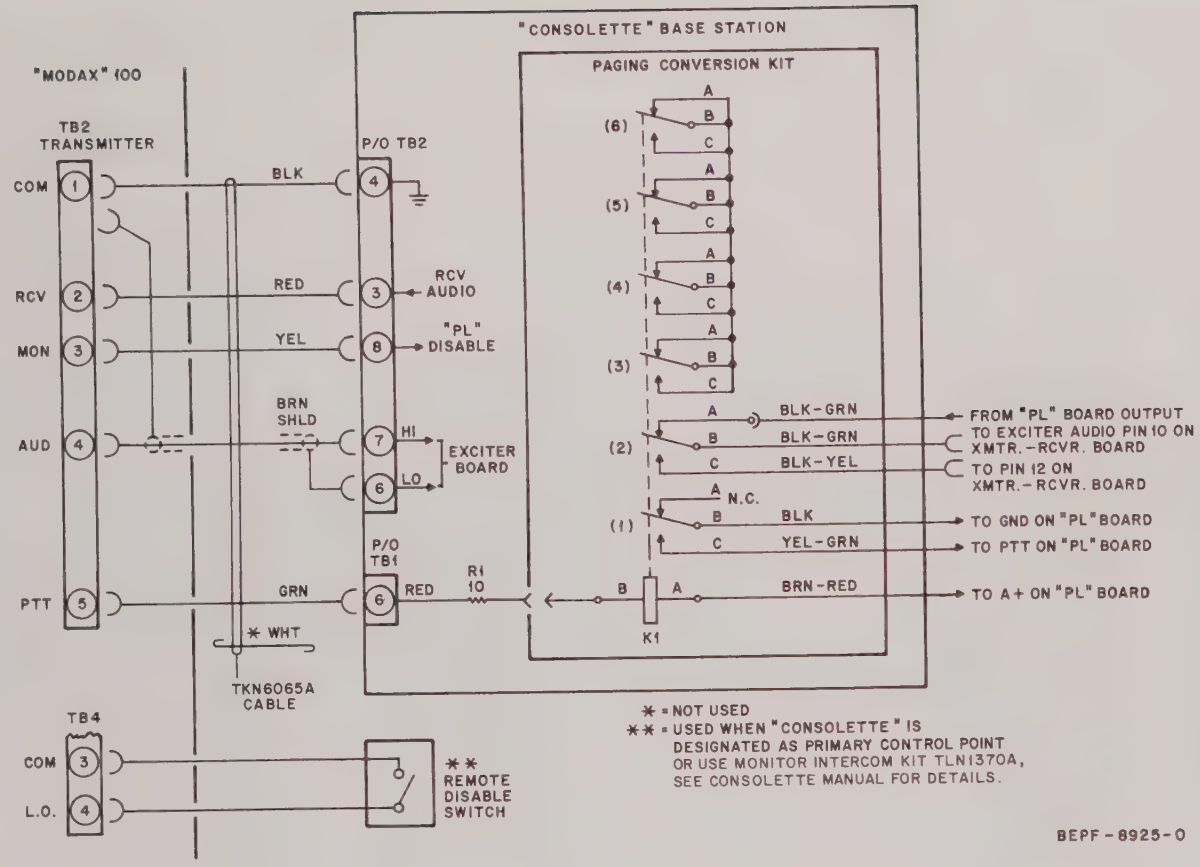


Figure 11. "Consolette" Base Station ("Private-Line") Connections

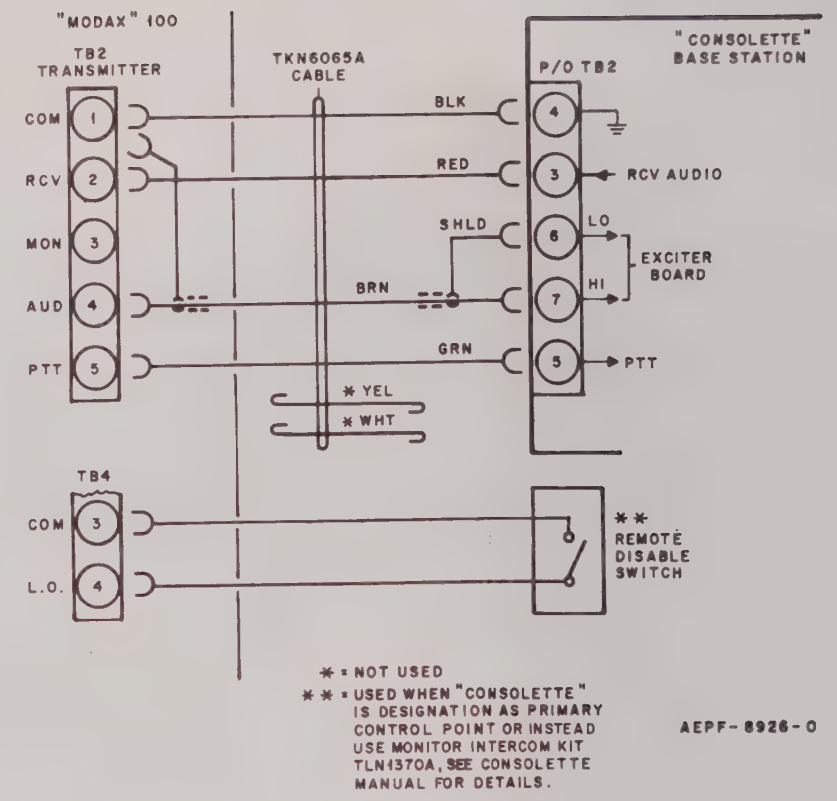


Figure 12. "Consolette" Base Station (Carrier Squelch) Connections

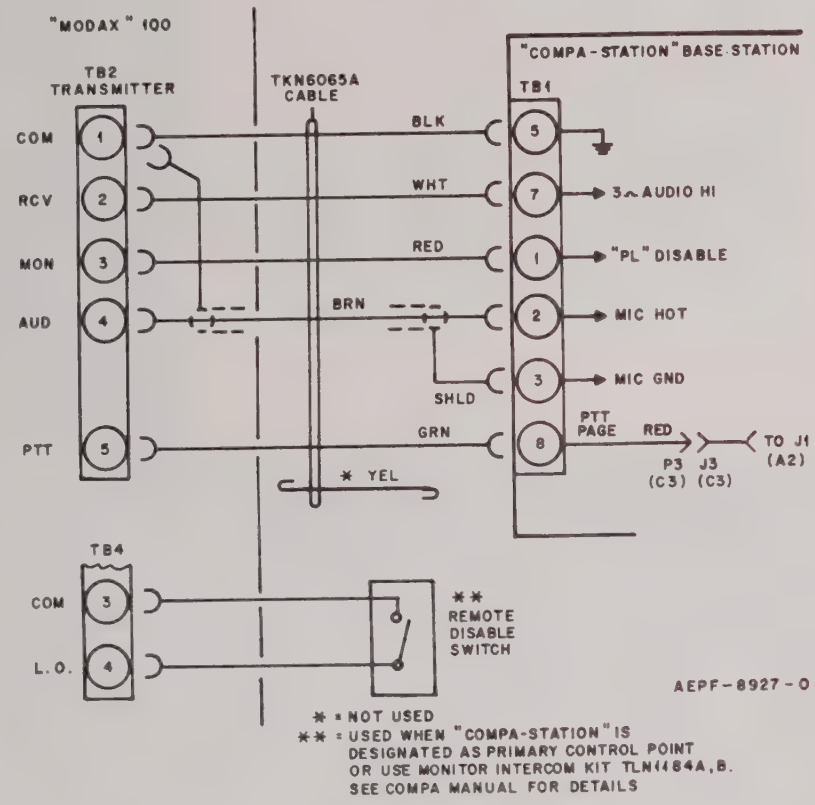


Figure 13. "Compa-Station" Base Station ("Private-Line") Connections

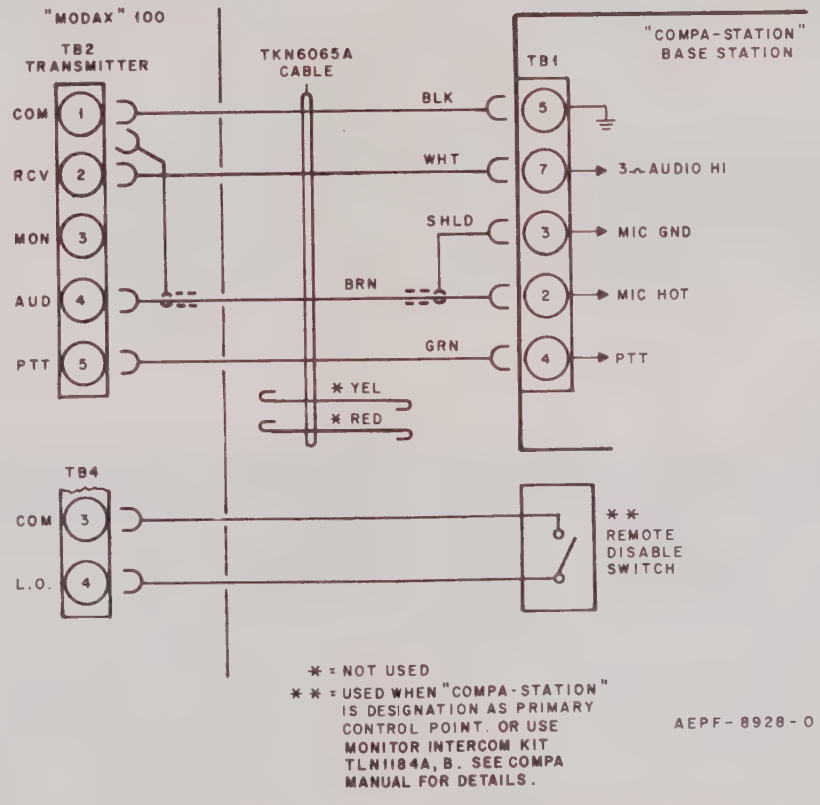


Figure 14. "Compa-Station" Base Station (Carrier Squelch) Connections

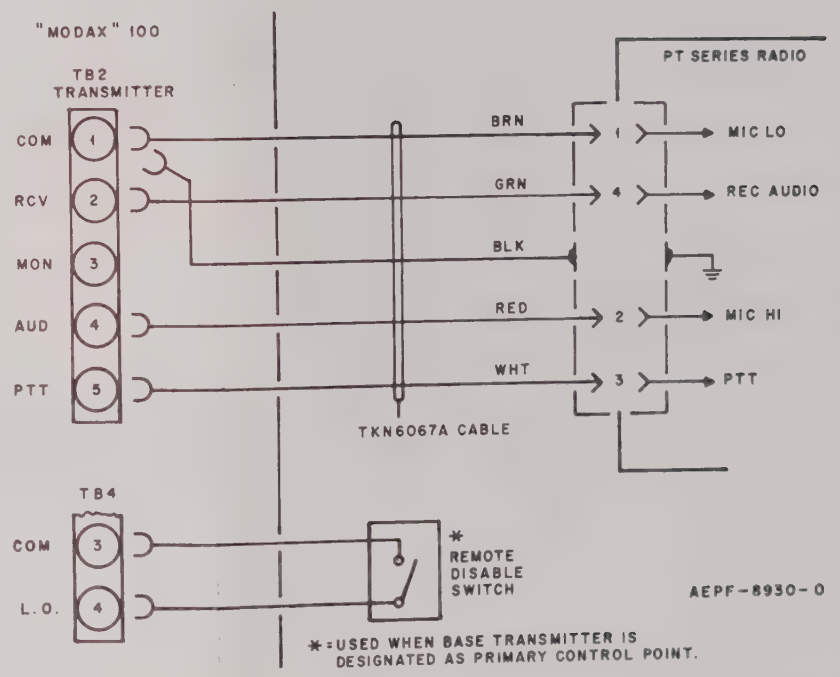
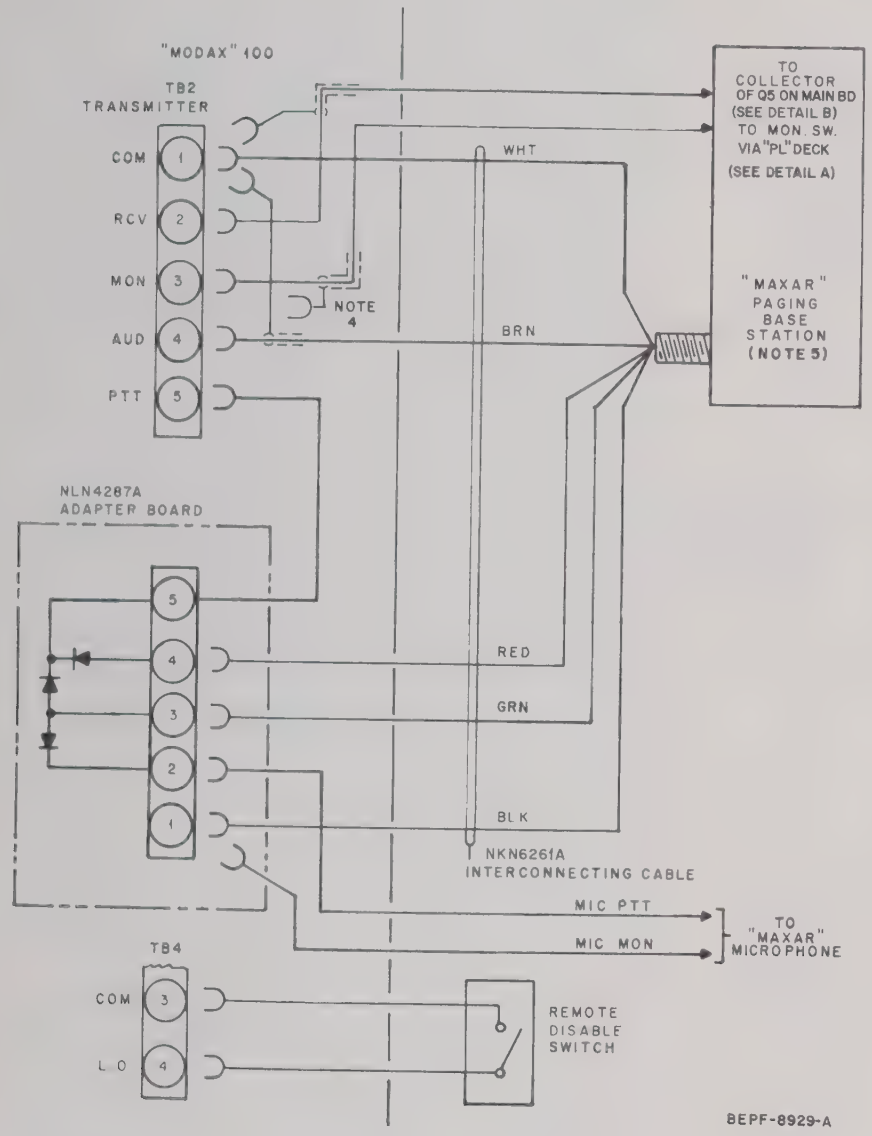
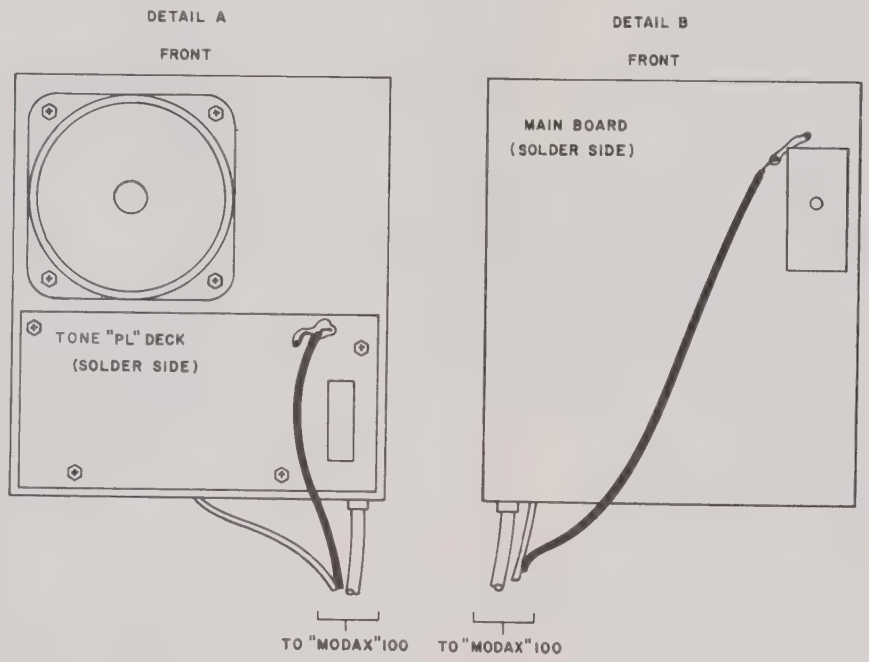


Figure 15. PT Series Base Station (Carrier Squelch) Connections



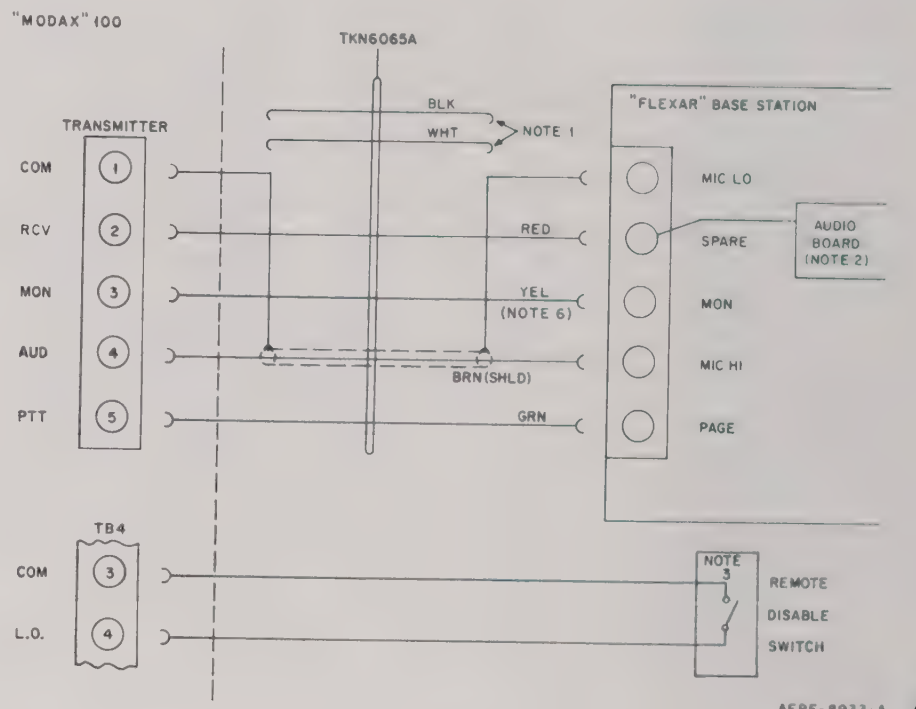


NOTES:

1. REMOTE DISABLE SWITCH USED WHEN "MAXAR" IS PRIMARY CONTROL POINT.
2. INTERCABLING SHOWN FOR "PL" SQUELCH FOR CARRIER SQUELCH, DELETE THE ADAPTER BOARD AND ATTACH THE GRN WIRE TO TB2-5. THE RED, BLK, AND MONITOR (TB2-3) WIRES ARE NOT USED.
3. THE ADAPTER BOARD MOUNTS DIRECTLY ON TB2 WITH THE SCREW TERMINAL DESIGNATIONS IN THE SAME SEQUENCE (5 OVER 5, 4 OVER 4, ETC.).
4. SHIELD CONNECTION NOT REQUIRED. LUG SHOULD BE TAPED TO CABLE.
5. CARRIER SQUELCH MODELS REQUIRE NKN6261A CABLE KIT. "PL" MODELS REQUIRE NLN1319A INTERFACE KIT WHICH INCLUDES TWO NKN6261A CABLE KITS AND THE NLN4287A ADAPTER BOARD.

EPF-8967-A

Figure 16. "Maxar" Base Station Connections



NOTES:

1. BLK AND WHT WIRES NOT USED.
2. CONNECT THE AUDIO OUTPUT FROM 3-WATT AUDIO BOARD TO SPARE TERMINAL ON REAR OF "FLEXAR".
3. REMOTE DISABLE SWITCH USED WHEN "FLEXAR" IS DESIGNATED AS PRIMARY CONTROL POINT.
4. THE INTERNAL SPEAKER IN THE "FLEXAR" SHOULD BE DISCONNECTED, IF THE "MODAX" TERMINAL IS THE CONTROL POINT.
5. THE "FLEXAR" VOLUME CONTROL AFFECTS THE RECEIVE AUDIO LEVEL HEARD FROM THE "MODAX" MONITOR SPEAKER.
6. MONITOR LINE (YELLOW WIRE) NOT USED WITH CARRIER SQUELCH STATIONS.

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Figure 17. "Flexar" Base Station Connections

NOTES:

1. REMOTE DISABLE SWITCH USED WHEN CONSOLE IS PRIMARY CONTROL POINT.
2. A NORMALLY CLOSED SWITCH IS REQUIRED TO MONITOR "MODAX" XMIT AUDIO. THE SWITCH MUST OPEN FOR MICROPHONE USE.
3. THE TLN6773A TRANSMIT INDICATOR KIT IS REQUIRED TO SATISFY FCC REGULATIONS.

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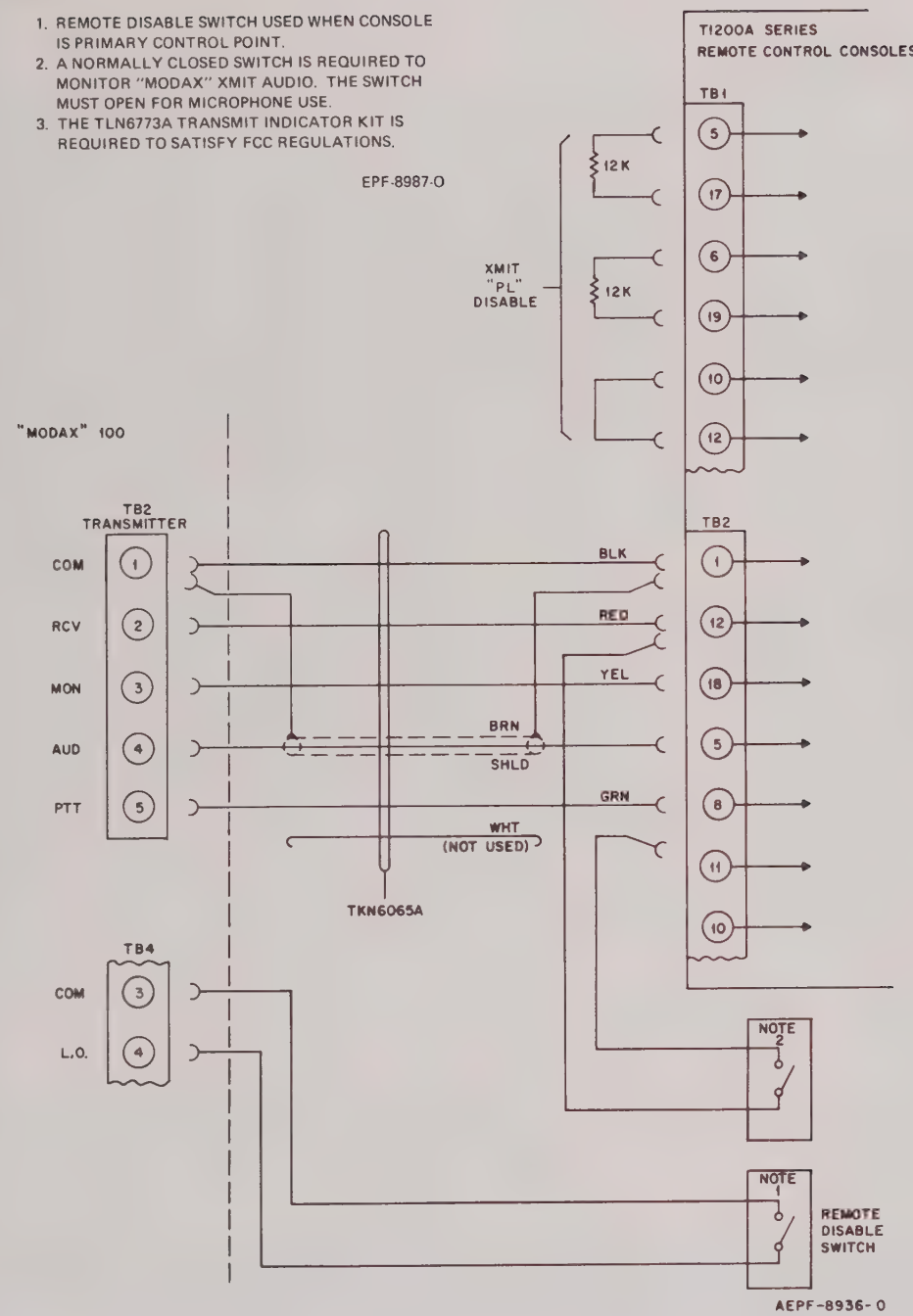
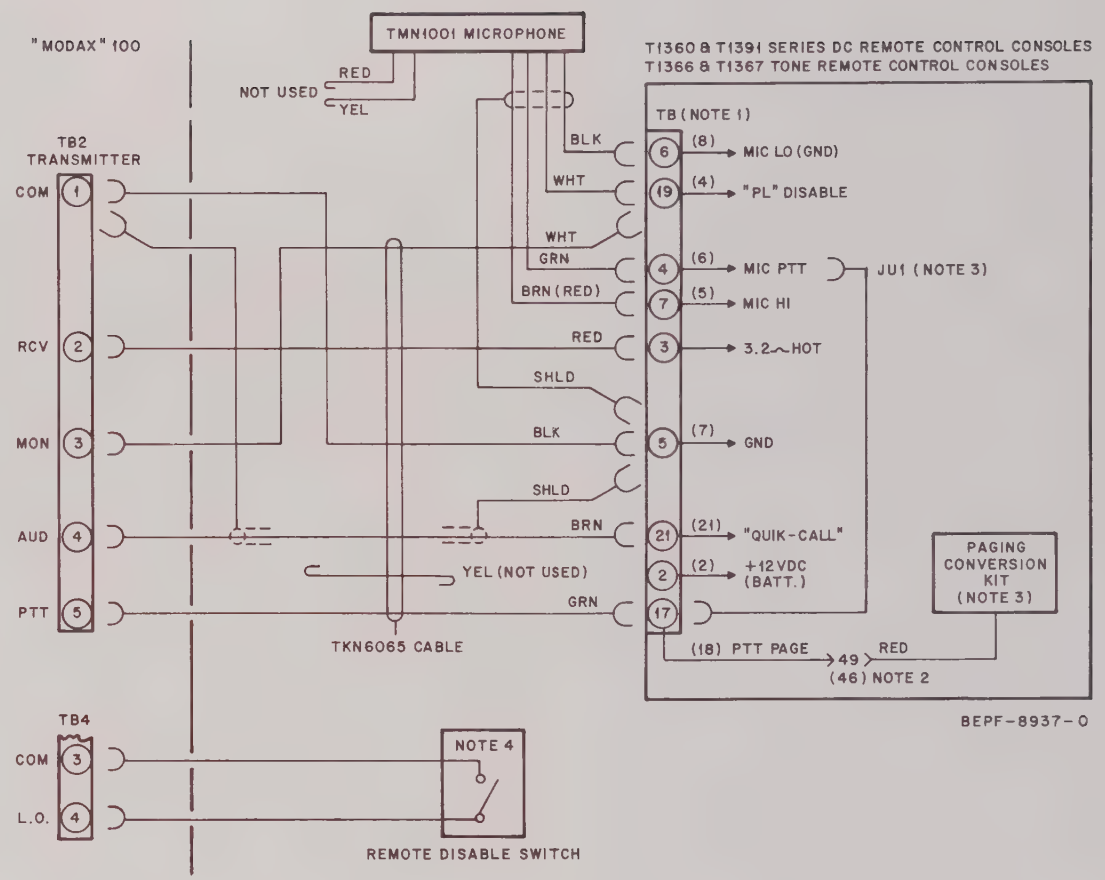


Figure 18. T1200 Series Console Connections



NOTES:

1. TB NUMBERS FOR T1360 SERIES CONSOLES ARE IN BRACKETS ( ).
2. CONNECTOR IS USED WHEN PAGING CONVERSION KIT IS FACTORY INSTALLED. JUMPER JU22 (A+ TO TB-17) ON THE T1391 SERIES CIRCUIT BORAD IS REMOVED WHEN THE CONVERSION KIT IS INSTALLED.
3. FOR CARRIER SQUELCH OPERATION, OMIT PAGING CONVERSION KIT AND ADD JUMPER JU1 FROM TB-17 TO TB-4 ON CONSOLE.
4. REMOTE DISABLE SWITCH USED WHEN CONSOLE IS CONTROL POINT.
5. CUT JU1 ON MIC BOARD FOR MIC POWER ON TRANSMIT ONLY.
6. CUT JU10 AND JU15 ON MAIN CONSOLE BOARD TO PREVENT MUTING THE SPEAKER ON TRANSMIT.

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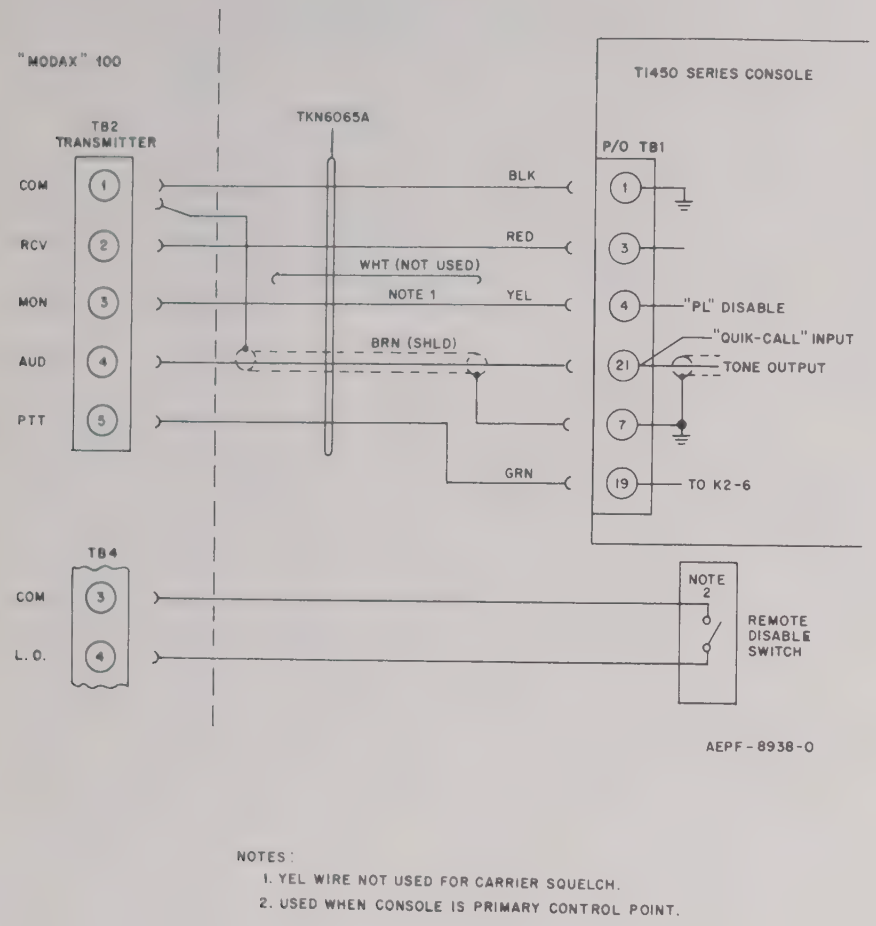
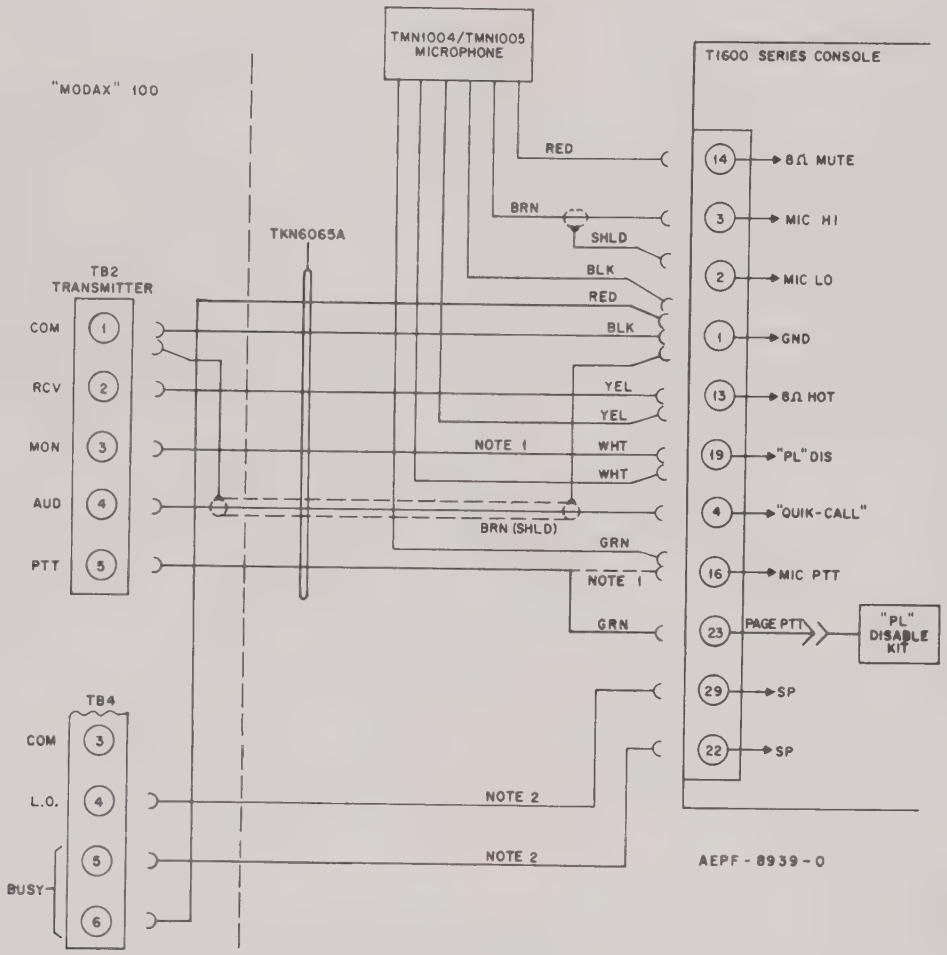
Figure 19. T1300 Series Console Connections



NOTES:

1. YEL WIRE NOT USED FOR CARRIER SQUELCH.
2. USED WHEN CONSOLE IS PRIMARY CONTROL POINT.

Figure 20. T1450 Series Console Connections



NOTES:

1. FOR CARRIER SQUELCH, GRN WIRE IS CONNECTED FROM TB2-5 TO T1600 TERMINAL 16 AND WHT WIRE FROM TB2-3 TO T1600 TERMINAL 19 IS NOT USED.
2. T1600 CONSOLE INCLUDES PAGING CONTROL KIT (TLN1501) CUT JU20 ON MAIN CONSOLE BOARD.
3. CUT JU1 ON MICROPHONE BOARD FOR MIC POWER ON TRANSMIT ONLY.
4. REMOVE DIODE CR2 ON PAGING CONTROL KIT AND CUT JUMPERS JU6 AND JU7 ON MAIN CONSOLE BOARD TO PREVENT MUTING THE SPEAKER ON TRANSMIT.

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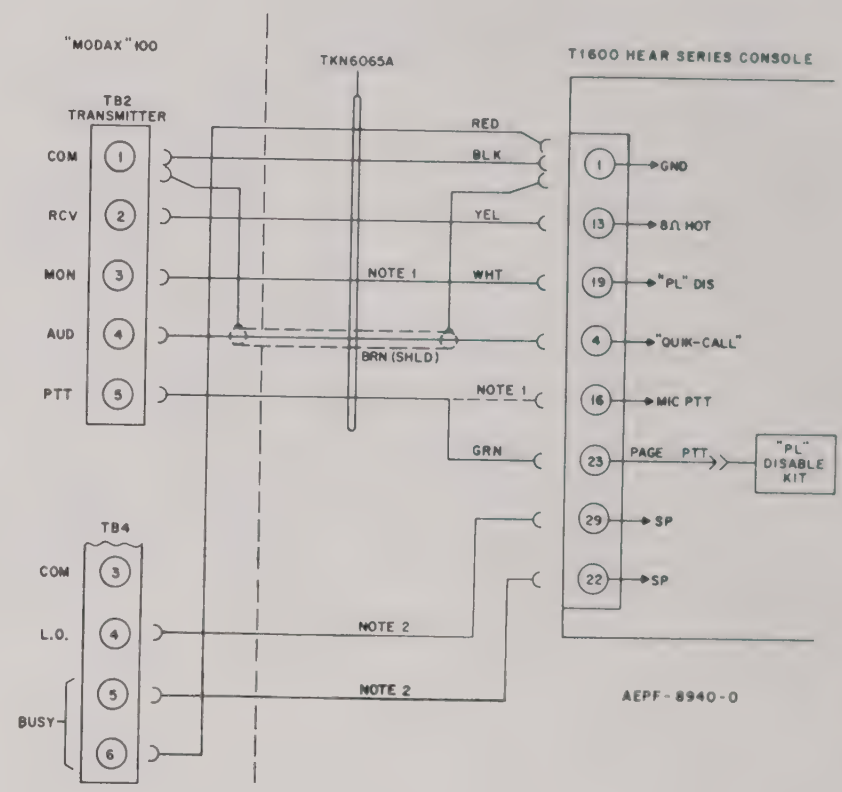
Figure 21. T1600 Series Console (DC & Tone) Connections



NOTES:

1. FOR CARRIER SQUELCH, GRN WIRE IS CONNECTED FROM TB2-5 TO T1600 TERMINAL 16 AND WHT WIRE FROM TB2-3 TO T1600 TERMINAL 19 IS NOT USED
2. T1600 CONSOLE INCLUDES PAGING CONTROL KIT (TLN1501) CUT JU20 ON MAIN CONSOLE BOARD.
3. REMOVE DIODE CR2 ON PAGING CONTROL KIT AND CUT JUMPERS JU6 AND JU7 ON MAIN CONSOLE BOARD TO PREVENT MUTING THE SPEAKER ON TRANSMIT

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Figure 22. T1600 Series Console (HEAR) Connections

(2) Subaudible Connections

Figures 23 and 24 illustrate typical interconnections between the paging terminal and the base station when subaudible paging operation is to be used. Figure 23 shows the connections required in a local control console setup using the NLN1130 Subaudible Interface Kit. Figure 24 shows connections for a remote control console setup using the SP57011801 Subaudible Remote Kit.

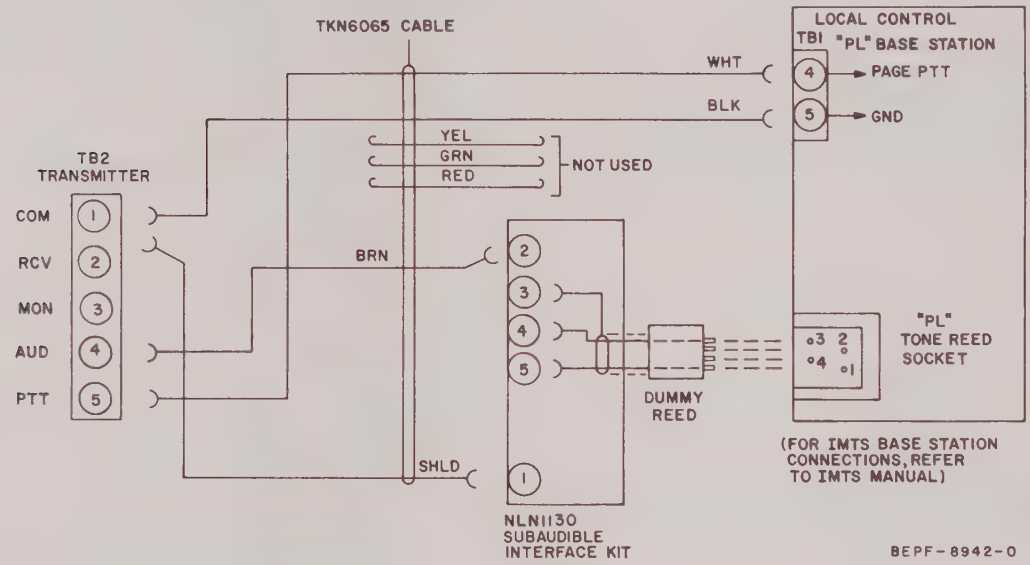

Figure 23. Subaudible Local Control Interconnections

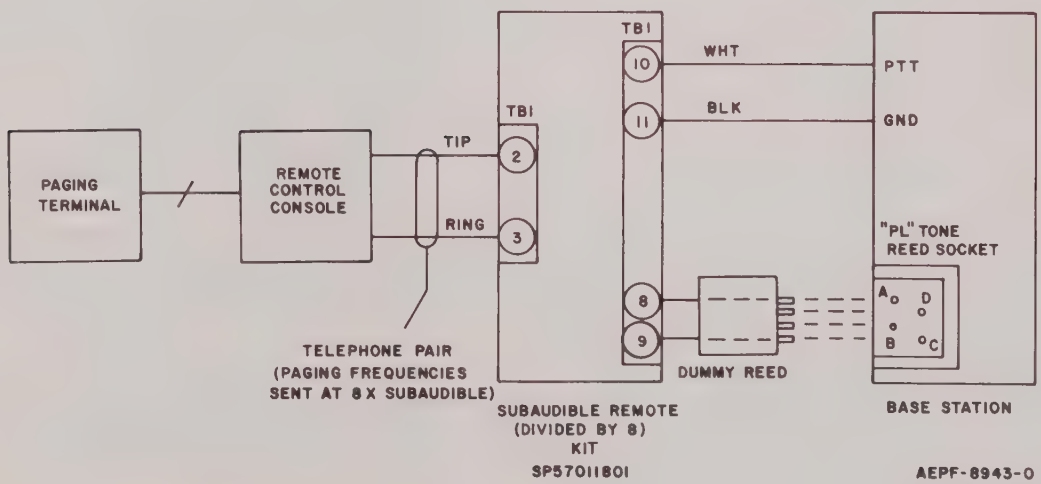

Figure 24. Subaudible Remote Control Interconnections

(3) Multiple Paging Terminals

Multiple terminals can be connected as shown in Figure 25. If more than two units are paralleled, the resistor coupling method cannot be used due to excessive loading. External relays or circuits are required for more than two units.

d. Battery Connections

When it is necessary to operate the terminal from a dc power source, a battery may be connected to the two-screw terminal strip (TB3) labeled 13.8 V BATTERY. Refer to Figure 26.

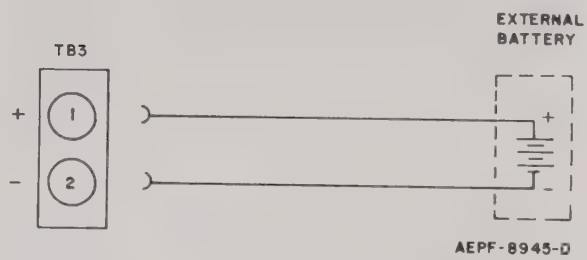

Figure 26. External Battery Connections

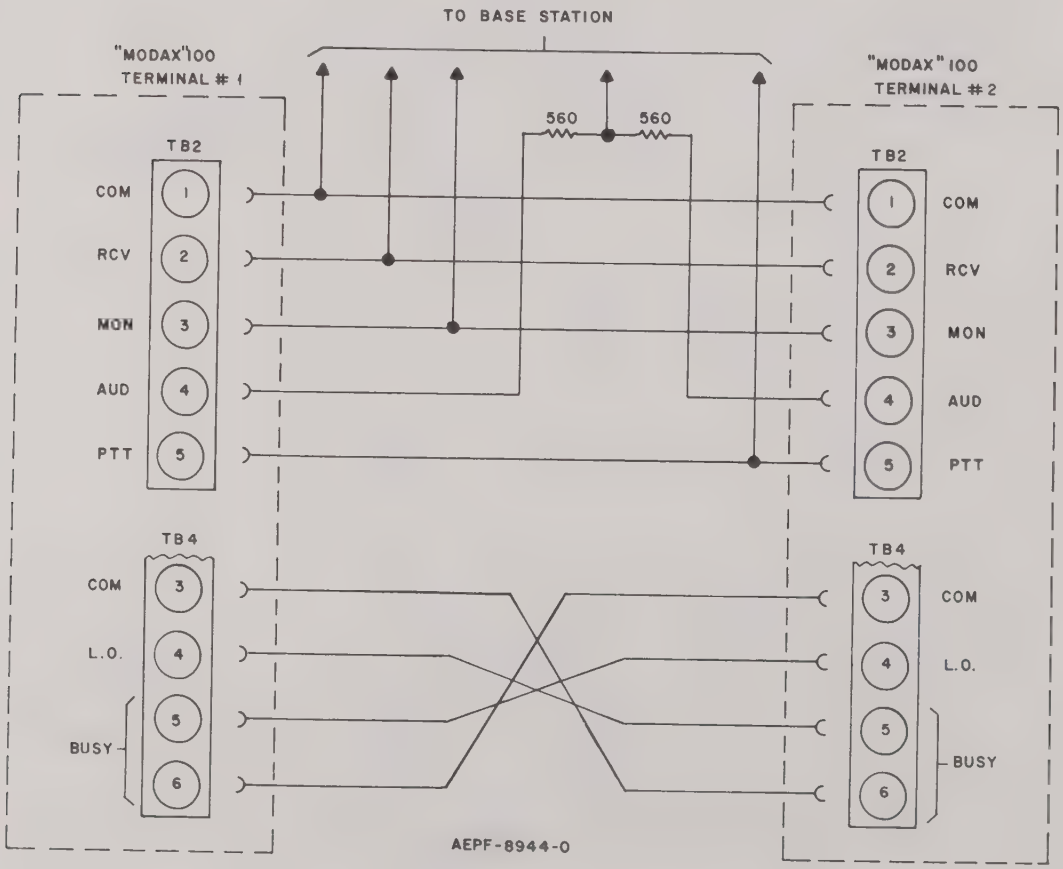

Figure 25. Multiple Paging Terminal Interconnections

e. Emergency Page Connections

Terminals equipped with the NLN5109A Main Circuit Board Kit have the capability of automatically paging two pagers when a simple contact closure is applied to an input (TB4) on the rear of the terminal. Connect the emergency page switches as shown in Figure 27. Refer to the instructions in the Setup Procedures section of the manual and set the emergency pager codes as desired.

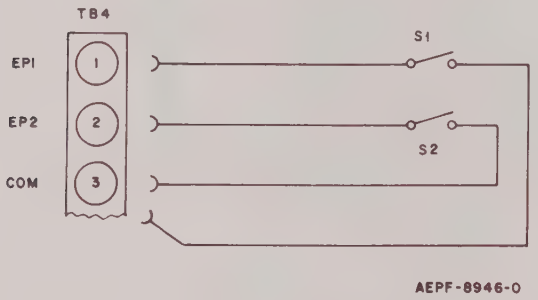

Figure 27. Emergency Page Connections

f. Telephone Company Connections

(1) Line Level Inputs

In an end-to-end system, the paging terminal is connected to the telephone line tip and ring, the same as an ordinary telephone. A cable terminated by a modular plug (standard USOC RJ11C) is provided for this connection.

NOTE

Some installations may require a modular plug to 4-prong adapter, available from the telephone company or local electronics supplier.

The cable is connected internally to two screws on the NLN5114A Line Level Protection Circuit (GRN = Tip and RED = Ring).

NOTE

The Disconnect Detector is polarity sensitive. If it does not work, reverse tip and ring and try again.

When an RDMZR Interface Unit is used in place of the NLN5114A Line Level Protection Circuit, the NKN6255A Adapter Cable is required. The cable connects to the rear of the paging terminal as shown in Figure 28.

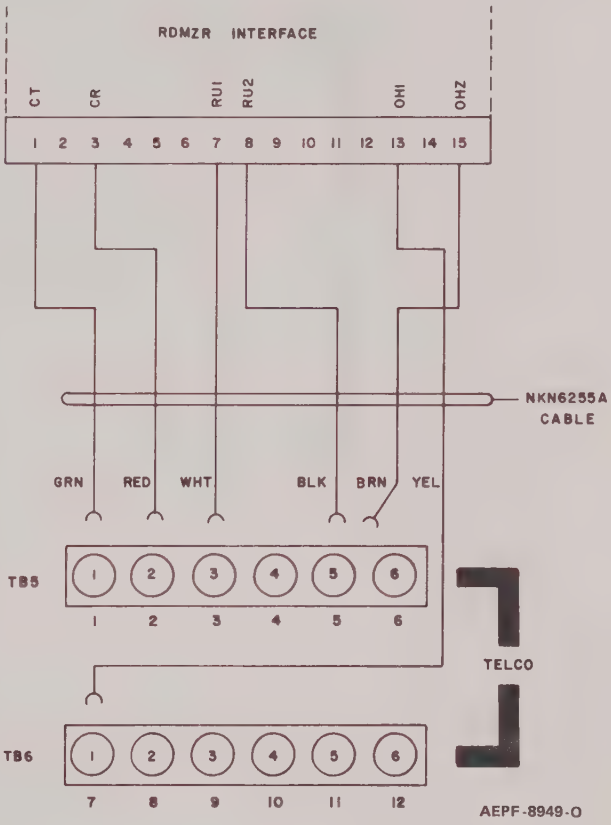

Figure 28. RDMZR Interface Connections

(2) Selector Level Inputs

In selector level systems, the telephone interface equipment is connected to the paging terminal via the two 6-screw terminals labeled TELCO. The terminal strips are referenced as TB5 and TB6, and the screw connections are marked 1 through 12. Not all connections are used in each installation, but vary depending on the type of telephone input and how the terminal is equipped. Figures 29, 30, and 31 show the DCK and DCW interface connections to the paging terminal and Figures 32 and 33 are simplified schematic diagrams of the telephone company equipment.

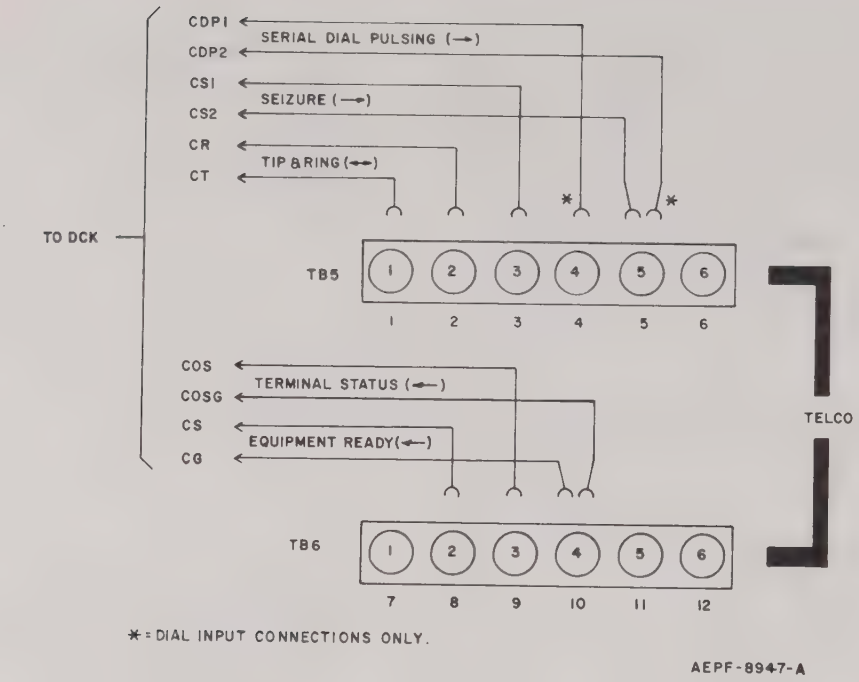

Figure 29. TELCO Connections to DCK

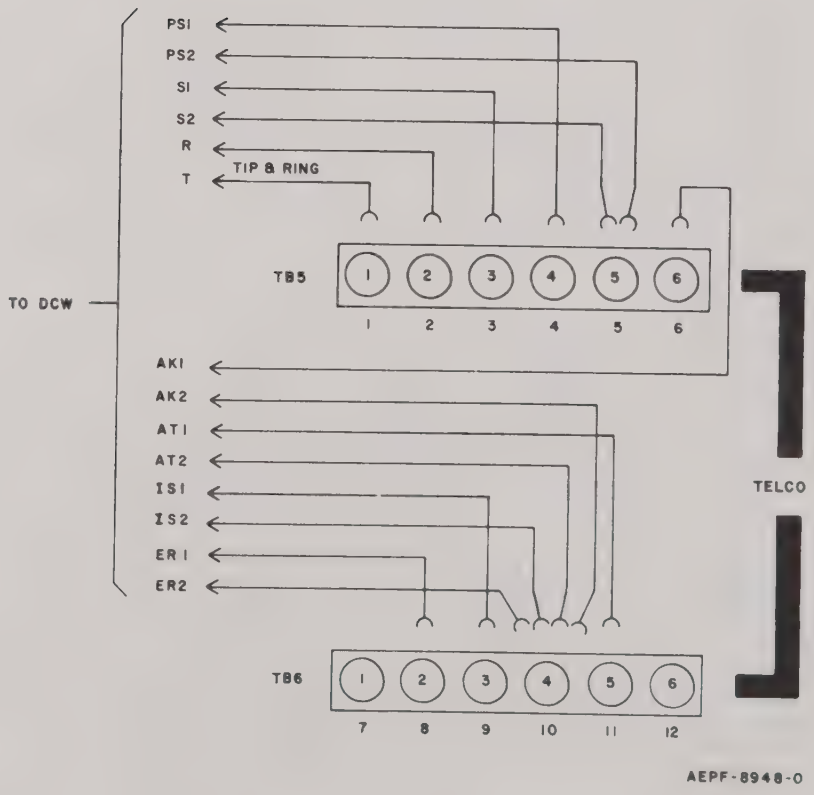

Figure 30. TELCO Connections to DCW (Dial Input)

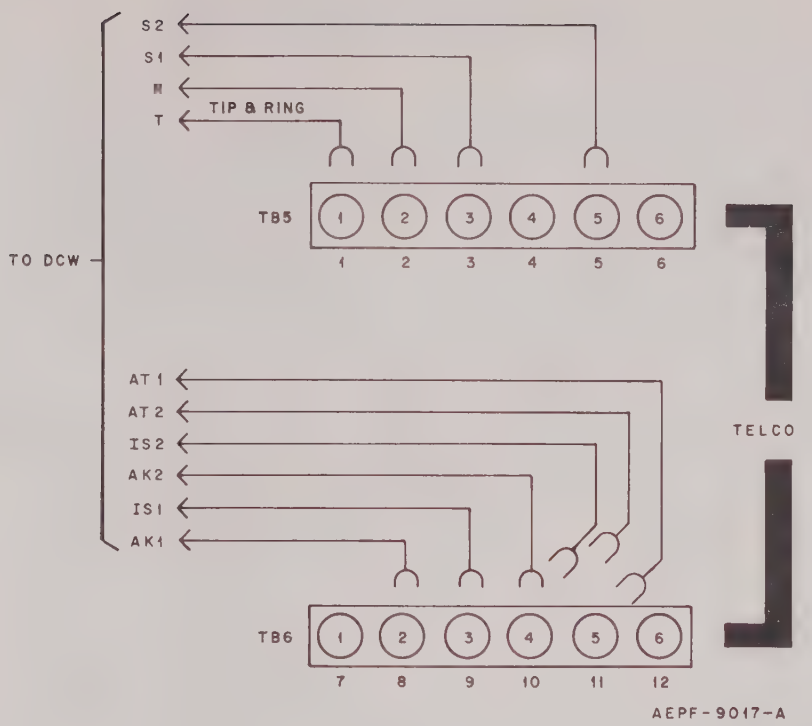

Figure 31. TELCO Connections to DCW (Tone Input)

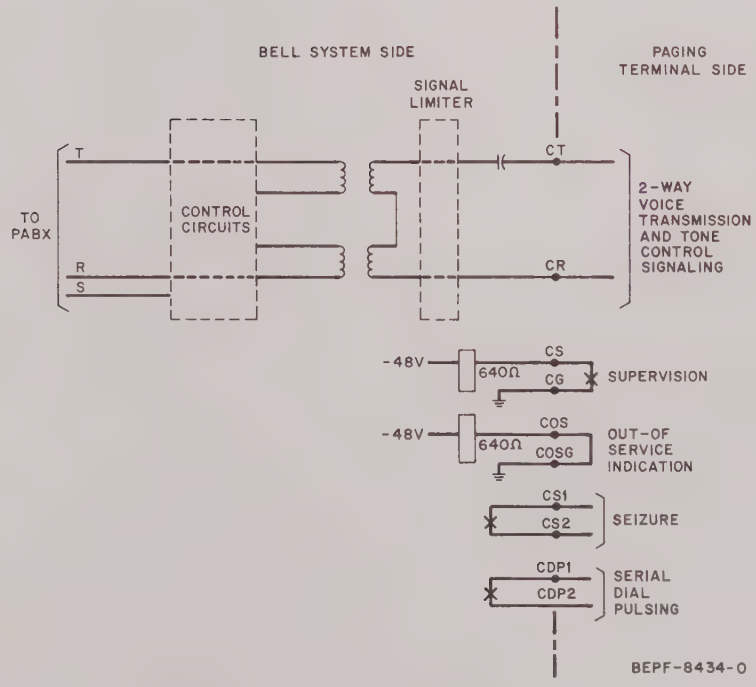

Figure 32. Simplified Schematic — Voice Connecting Arrangement DCK

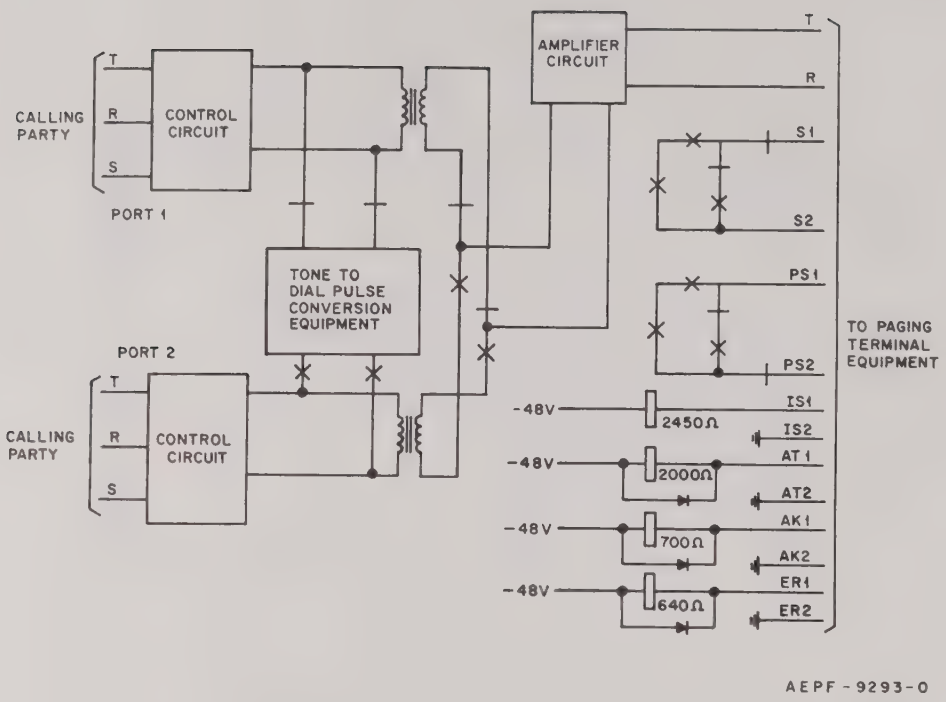

Figure 33. Simplified Schematic — Voice Connecting Arrangement DCW

g. COR Connections

The only connection unique to two-way operation is the TELCO terminal (TB6-6) labeled 12 on the rear panel.

This connection is used only with base stations equipped with a carrier-operated-relay (COR) that provides a closure when a received rf carrier is detected. This relay closure produces the signal COR, which is used on the two-way board to control the operating mode (transmit or receive) of the terminal. The base station relay is connected to the terminal as shown in Figure 34.

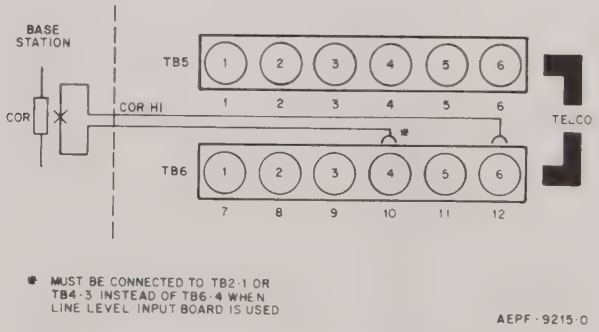

Figure 34. COR Connections

SETUP PROCEDURES

1. GENERAL

This section contains the post installation setup procedures and initial adjustments required prior to operating the terminal on-line in a fully functional system. Due to the flexibility of the equipment, the procedures required will vary depending on the particular installation. All variations are given and those procedures that apply to your installation should be selected.

Preoperational adjustments and level settings are described where required with resistor value changes given when necessary.

Special procedures are also given for inactivating a pager code, and for substituting an alternate pager code. These functions are available in terminals equipped with the Universal Number Interchange (UNI) feature, and are easily identified by the special front panel with the digital readout.

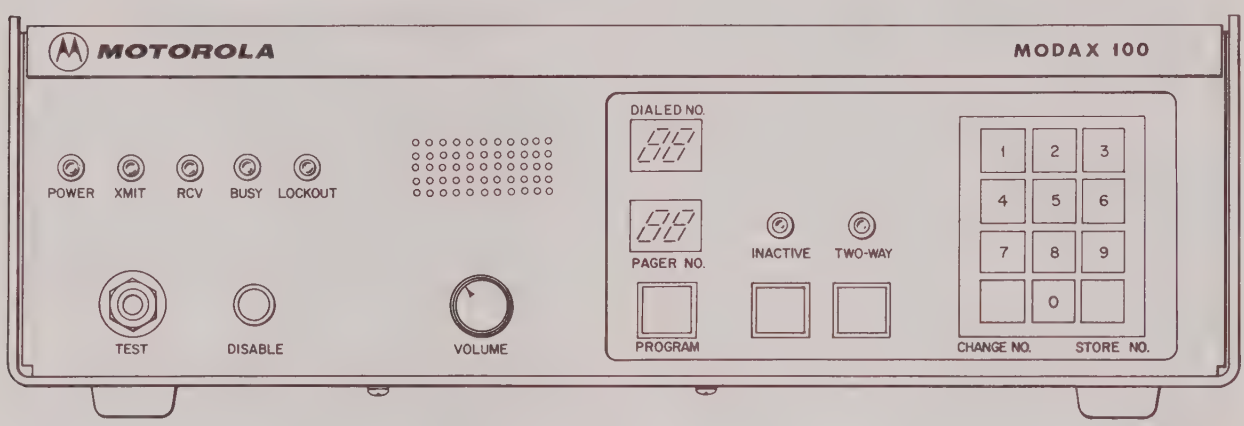

Figure 35. "MODAX" 100 Front Panel

BEPF-8798-0

2. FRONT PANEL CONTROLS AND INDICATORS

PANEL MARKING	DESCRIPTION	FUNCTION
POWER	Indicator, LED	Glows when ac or dc power is applied to the terminal.
XMIT	Indicator, LED	Glows when terminal output is provided to the transmitter.
RCV	Indicator, LED	Glows when terminal audio is monitored at remote control point.
BUSY	Indicator, LED	Glows when terminal is accessed.
LOCKOUT	Indicator, LED	Glows when terminal is locked out due to priority, emergency page, or the UNI circuit is activated.
TEST	Telephone Jack	Used for test telephone connection.
DISABLE	Pushbutton Switch	Used to terminate a page in process on Dial-up Network.
VOLUME	Control	Used to adjust the audio level for local monitoring.
DIALED NO.	Two-digit display	Indicates the dialed pager code.
PAGER NO.	Two-digit display	Indicates the transmitted pager code.
PROGRAM	Pushbutton Switch	When held depressed, enables the UNI panel switches and keyboard. Lockout terminal input.
INACTIVE	Indicator, LED	Glows when dialed number is inactive.
INACTIVE	Pushbutton Switch	Used to activate or inactivate the pager code in the DIALED NO. window.
* TWO-WAY	Indicator, LED	Glows when dialed number is programmed for two-way operation.
* TWO-WAY	Pushbutton Switch	Used to program the pager code in the DIALED NO. window for two-way operation.
1, 2, 3, 4, 5, 6, 7, 8, 9, 0	Keyboard Switches	Used to enter pager codes.
CHANGE NO.	Keyboard Switch	Used to change the pager code in the DIALED NO. window.
STORE NO.	Keyboard Switch	Used to store the programmed conditions selected by the other switches on the UNI panel.

NOTE: If static discharge through keyboard causes system to lock up, turn power off and back on to reset system.

* Not functional without two-way option

3. AUDIO LEVEL ADJUSTMENTS

Before operating the system, the terminal transmit, receive, and monitor speaker audio levels must be adjusted. With power applied to the unit, raise the top cover, connect a telephone to the TEST jack on the front panel, and proceed as follows:

a. Transmit Audio Level

From the label on the bottom of the paging terminal, determine the tone group or specific frequencies that have been coded into the paging encoder. If a tone group is specified, refer to the "Tone Coding" section for the specific tone group table listing the specific frequencies for that particular tone group. If a particular tone group was not used, then the label on the bottom of the paging encoder should list the specific frequencies for its associated digit.

From the tone group frequencies, choose the highest, lowest, and middle range frequencies; note the corresponding digits. For example, for tone group one, the highest frequency is 539.0 Hz and the lowest frequency is 330.5 Hz. The middle range of the highest and lowest frequencies is derived by subtracting the lowest frequency from the highest frequency, dividing by two, and adding the answer to the lowest frequency or subtracting it from the highest frequency:

Let LF = Lowest Frequency,
MF = Middle Frequency,
HF = Highest Frequency;

$$MF = \frac{HF - LF}{2} + LF \quad \text{or} \quad MF = HF - \frac{HF - LF}{2}.$$

After deriving the middle frequency of the tone group, determine which tone frequency is closest to the calculated middle frequency. Using the preceding example, the middle frequency of tone group one should have been calculated to be 434.75 Hz. Checking the tone group one table, 433.7 Hz is the closest frequency to the calculated middle frequency. Therefore, for tone group one, 0 produces the lowest frequency, 5 produces the middle frequency, and 9 produces the highest frequency. For tone group three, after selecting the lowest frequency and highest frequency and calculating the middle frequency, we find that 1 produces the lowest frequency, 5 produces the middle frequency, and 0 produces the highest frequency. The lowest, middle, and highest frequencies of each tone group can be determined in the preceding manner.

Refer to Figure 36 and the main terminal circuit board and locate the A, HALT, and B test points (near U31 and U32). Jumper HALT to A (HALT is the center post), and tone A, the left-hand digit of the display, will be generated until the jumper is removed.

Figure 36. Tone B Jumper Placement

Enter the digit corresponding to the middle frequency of the tone group via the test telephone dial and, using a service monitor at the transmitter site, adjust potentiometer R133 for a frequency deviation of ±3.3 kHz.

Enter the high and low frequencies of the paging encoder and record their readings in the same manner as done for the middle frequency.

NOTE

A deviation of ±3.3 kHz is a typical setting (±0.75 kHz for subaudible). It is recommended that the appropriate pager manual be consulted for proper deviation settings. For further information, refer to Service and Repair Notes Bulletin SRN-514, August 1974.

Adjust the deviation (R133) such that the worst reading is ±3.3 kHz. Also ensure that the highest reading is not displaying a clipped waveform on the service monitor. If ±3.3 kHz cannot be attained or a clipped waveform is shown when setting for a minimum of ±3.3 kHz, adjust R133 for a minimum setting of ±2 kHz. If ±2 kHz cannot be attained, continue to the following paragraph.

If a minimum deviation of ±2 kHz cannot be attained and the frequencies are correct, it could be that the terminal is not providing sufficient signal to the base station. Typically, the base station requires .165 volt rms for 60% or ±3.0 kHz deviation. The "MODAX" 100 terminal provides a de-emphasized (6 dB/octave) paging tone to the base station. If the generated frequencies are 2 kHz or greater, then capacitor C23 (.068 uF) may have to be removed. The paging tones will then be fed to the base station "flat." The de-emphasis characteristic of capacitor C23 is necessary to offset the base station pre-emphasis characteristic, but if in the group of frequencies to be generated there exists less than

an octave difference, de-emphasis is not necessary. If the terminal is supplying sufficient signal to the base station, consult the signal and adjustment section of the base station instruction manual. If remote is used, keep audio level at -8 dB maximum or below knee of compression.

Dial the digit corresponding to the frequency closest to 1 kHz and measure the voltage at pin 3 (ORG wire) on the speaker amplifier board and note this reading for future use. Remove the HALT jumper.

b. Receive Audio Level

Using the service monitor, transmit a signal to the base station receiver with a 1 kHz tone at 5 kHz deviation. Monitor the wiper of potentiometer R136 on the main terminal board and adjust R136 for +6 dBm. This results in a -10 dBm average voice level to the telephone line.

c. Monitor Speaker Audio Level

With the service monitor transmitting the 1 kHz tone, adjust R1 on the speaker amplifier board to match the reading noted while adjusting transmitter audio level (pin 3 - ORG wire).

4. LINE LEVEL DIAL DIGIT DETECTION ADJUSTMENT NLN5110A

After the paging system is installed, a jumper implemented adjustment is required for digit detection. Locate jumper JU1 (pin 1 of U21) on the input board and connect it to pin 1 (R12). Using a telephone in the PABX system, dial the terminal access code.

NOTE

There will be a delay of approximately 4 to 5 seconds before the go-ahead tone is returned.

After the go-ahead tone is received, enter the following digits:

a. "00" for units equipped with the UNI digit display.

b. A subscriber number that contains a "0" ("9" if "0" is not available, "8" if no "9," etc.) if the digit display is not available.

If the dialed digits are properly accepted (correct digits displayed or correct pager signalled), repage this number several times.

If the dialed number is not correctly received, change jumper JU1 to pin 2 (R11) and repeat the test. Continue to pins 3 (R10) and 4 (R9) if the lower number pin does not work.

When JU1 is connected to the lowest pin number that will accept the digits correctly, move it to the next higher pin number and redial the digits. After the paging tones have completed, speak loudly into the telephone. If the loud voice input does not prematurely dump the call (before regular time-out occurs), use this setting. If voice does cause dumping, return JU1 to the next lower pin number and use that setting.

NOTE

Any mechanical shock to the phone could possibly cause a disconnect and should be considered normal operation.

5. ALLOTMENT TIMER SETTING

Each of the four input boards available contains an allotment timer circuit, which controls the maximum time allotted for the caller to deliver his voice message during a tone and voice page. The time is nominally set for 14 seconds at the factory. If a longer or shorter allotment time is desired, resistor R82 on the tone input boards or R52 on the dial input boards may be increased or decreased in value.

The factory installed value is 1.2 megohms for 14 seconds. If the value is doubled, the allotment time will double. If the value is halved, the allotment time will be cut in half. The value of R82 or R52 should not exceed 5 megohms.

6. ASI TIMING SETTING

The ASI is sent automatically 25 minutes after a page is transmitted. Due to FCC regulations in some localities, however, the ASI must be sent every 15 minutes. In order to meet the FCC regulations in the designated localities, resistor R116 (located between U40 and U41 on the main terminal circuit board) should be changed from 560 k to 270 k.

7. TONE TIMING RESISTORS

Depending upon the order, the paging terminal is shipped from the factory with the tone timing set for tone-only or tone-and-voice operation. Table 22 lists resistors and values that are changed according to the timing desired.

The times shown in Table 22 are the times required by the paging receiver. In tone remote control systems, the RC time constant should account for the 200 milliseconds that tone A is muted while the transmitter turn-on tones are being sent.

Table 22. Tone Timing Resistor Values

SIGNALING MODE	RESISTOR THAT TIMING IS DEPENDENT ON				
	TONE A			TONE B	
	TONE LENGTH (MINIMUM)	RESISTOR VALUE		TONE LENGTH (MINIMUM)	RESISTOR VALUE
		R28	R29		R31
Tone-and-Voice	1.0 sec.	120 k	390 k	3.0 sec.	220 k
Tone-Only	.4 sec.	47 k	560 k	.8 sec.	68 k
Tone-Only with Battery Saver	2.7 sec.	390 k	560 k	.8 sec.	68 k
Subaudible	1.0 sec.	120 k	390 k	3.0 sec.	220 k

NOTE: Formulas for calculating tone timing are as follows:

$$\text{Tone A Timing} = 1.1 \left(\frac{R28 \cdot R29}{R28 + R29} \right) C8$$

$$\text{Tone B Timing} = 1.1\ (R31)\ C9$$

$$\text{Group Call Timing} = 1.1\ [R29\ (C8) + R31\ (C9)]\ (8s \text{ minimum})$$

8. SETTING EMERGENCY PAGER NUMBERS

There are two emergency pager numbers provided when the terminal is equipped with the NLN5109A main circuit board. A two-digit pager code for each pager is determined by the binary setting of the rocker switches (S1 and S2) on the circuit board. These switches are physically located at the upper left corner of the board.

Figure 37 shows S1 and S2 set for pager numbers 25 and 69, respectively. Note that on each switch, the four positions on the left (1 through 4) select the units or least significant digit of the pager code, and the four positions on the right (5 through 8) select the tens or most significant digit.

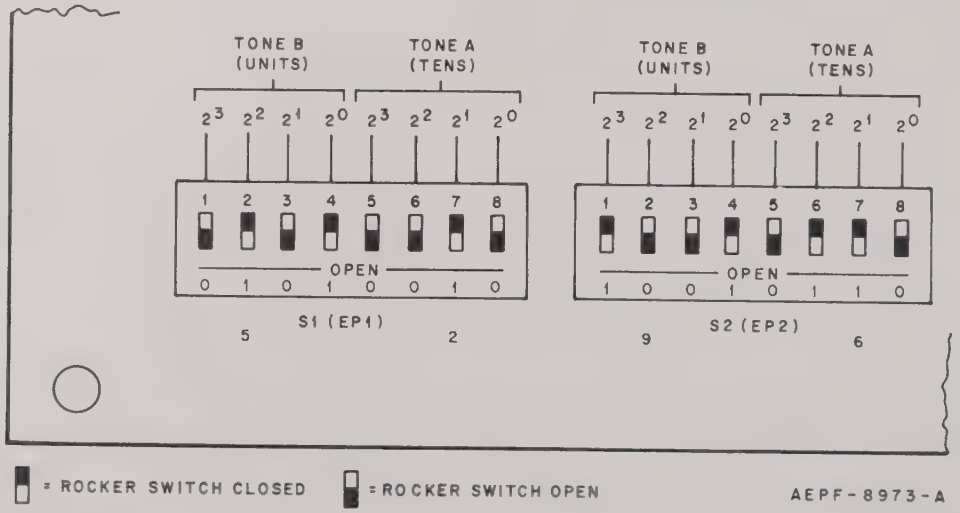

Figure 37. Emergency Pager Switches

9. JUMPER PLACEMENT OPTIONS

The following charts show standard jumper settings for a terminal as it is shipped from the factory.

a. Dial Pulse Input Boards

SELECTOR LEVEL (NLN5111A)		
JUMPER	FROM	TO
JU1	NOT USED	
JU2	1	C
JU3	NOT USED	
JU4	2	C
JU5	NOT USED	
JU6	1	C
JU7	IN	
---	U21-11	U21-14
---	U13-5	U13-7
---	U13-9	U13-7
---	U6-1	U6-7

LINE LEVEL (NLN5110A)		
JUMPER	FROM	TO
JU1	U21-1	*
JU2	2	C
JU3	1	C
JU4	1	C
JU5	IN	
JU6	1	C
JU7	NOT USED	
---	T1 (BLU)	T1 (YEL)
---	T1 (BRN)	T1 (ORG)

* Refer to Digit Detection Adjustment Paragraph

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b. Tone Input Boards

SELECTOR LEVEL (NLN5113A)		
JUMPER	FROM	TO
JU1	IN	
JU2	1	C
JU3	1	C

LINE LEVEL (NLN5112A)		
JUMPER	FROM	TO
JU1	NOT USED	
JU2	2	C
JU3	1	C
---	T1 (BLU)	T1 (YEL)
---	T1 (BRN)	T1 (ORG)

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c. Main Terminal Boards

WITHOUT EMERGENCY (NLN5108A)		
JUMPER	FROM	TO
JU1	NOT USED	
JU2	NOT USED	
JU3	2	C
*JU3	1	C
---	U8-7	U34-11
---	U26-15	U26-13
---	U26-2	U26-12
---	U26-4	U26-11
---	U26-6	U26-10
---	U25-15	U25-13
---	U25-2	U25-12
---	U25-4	U25-11
---	U25-6	U25-10
---	U39-9	U39-7 GND
---	U39-5	U39-7 GND

WITH EMERGENCY (NLN5109A)		
JUMPER	FROM	TO
JU1	NOT USED	
JU2	NOT USED	
JU3	2	C
*JU3	1	C
---	U8-7	U34-11

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* Setting for systems with NO ASI.

--- represents jumpers not designated.

10. TEST PAGING PROCEDURE

Using a telephone in the PABX system, make a test paging call. Observe the terminal panel and check the normal events as follows:

a. Lift the Telephone Off-Hook

A dial tone will be heard.

b. Dial the Terminal Access Code

(1) Line Level - Ring-back will be heard until the terminal answers the line, BUSY lamp on, after a 3-second billing delay a "go-ahead" tone will be heard.

(2) Selector Level - BUSY lamp on, shortly after the terminal answers the line a "go-ahead" tone will be heard.

c. Dial a Two-Digit Pager Code

(1) The RCV lamp will light momentarily.

(2) The XMIT lamp will light.

(3) The two-digit code will appear in the DIALED NO. window.

(4) The two-digit code (or alternate) will appear in the PAGER NO. window.

(5) An "acknowledge" tone (beeping) will be heard for approximately four to eight seconds.

NOTE

The talk period now exists for about 15 seconds.

d. Listen for the Allotment Timer

A busy tone will be heard after about 15 seconds (nominal) when the allotment timer times out (DCW only).

e. Hang Up the Telephone

Repeat steps a and b before proceeding.

f. Dial an Invalid Pager Code (If equipped with UNI)

You will hear an invalid warble tone in the receiver.

g. Hang Up the Telephone

All lamps (indicators) on the front panel will go out, except the POWER lamp.

11. TEST PAGING PROCEDURE (Two-Way Radios)

Using a telephone in the PABX system, make a test paging call. Observe the terminal panel and check the normal events as follows:

a. Lift the Telephone Off-Hook

A dial tone will be heard.

b. Dial the Terminal Access Code

(1) Line Level - Ring-back will be heard until the terminal answers the line, BUSY lamp on, after a 3-second billing delay a "go-ahead" tone will be heard.

(2) Selector Level - BUSY lamp on, shortly after the terminal answers the line a "go-ahead" tone will be heard.

c. Dial a Two-Digit Pager Code (which is set for Two-Way Operation)

(1) The TWO-WAY lamp will light.

(2) The RCV lamp will light momentarily.

(3) The XMIT lamp will light.

(4) The two-digit code will appear in the DIALED NO. window.

(5) The Two-digit code (or alternate) will appear in the PAGER NO. window.

(6) An "acknowledge" tone (beeping) will be heard for approximately four to eight seconds.

NOTE

A two-way conversation period now exists for approximately one minute, unless jumper JU2 has been installed on the two-way board to change the allotment time.

d. Speak Into the Telephone

If a five-second period of silence is detected before the allotment timer times out, the call will be terminated with no indication to the caller.

If a conversation is maintained for the allotted period, a warning signal similar to the go-ahead tone will be heard ten seconds before the call is terminated.

e. Hang Up the Telephone

All lamps (indicators) on the front panel will go out, except the POWER lamp.

12. PRIORITY TELEPHONE TEST

Place a call on the priority telephone, with the transmitter disconnected, and observe the normal events as follows:

a. Lift the Telephone Off-Hook

The BUSY lamp will light and a "go-ahead" tone will be heard.

b. Dial a Two-Digit Pager Code

(1) The RCV lamp will light momentarily.

(2) The XMIT lamp will light.

(3) The two-digit code will appear in the DIALED NO. window.

(4) The two-digit code (or alternate) will appear in the PAGER NO. window.

(5) An "acknowledge" tone (beeping) will be heard until the paging tones are transmitted.

c. Hang Up the Telephone

The priority telephone has no allotment time.

13. PAGER STATUS CHECK PROCEDURE

STEP	PROCEDURE
1	Press and hold the PROGRAM button.
2	Observe that two decimal points appear in the DIALED NO. window.
3	Enter the two-digit pager code by pressing the proper numbers on the keyset.
4	Observe the front panel: a. If the INACTIVE lamp glows, the pager is inactive. b. If the TWO-WAY lamp glows, the pager is programmed for two-way radio operation (Selective-Call). c. If a different two-digit pager code appears in the PAGER NO. display, then a substitute pager number is programmed for the dialed pager code and the tones for the code in the PAGER NO. window will be transmitted.
5	Release the PROGRAM button.

14. PROCEDURE TO CHANGE ONE-WAY/TWO-WAY STATUS

The following table lists the steps required to perform the status change procedure:

STEP	PROCEDURE
1	Press and hold the PROGRAM button.
2	Observe that two decimal points appear in the DIALED NO. window.
3	Using the keyset, enter the two-digit code for the radio that you want to operate.
4	Observe that the DIALED NO. display indicates the correct code.
5	Observe the TWO-WAY indicator. A lighted lamp indicates two-way status. An unlit lamp indicates one-way status.
6	Momentarily press the CHANGE NO. button.
7	Observe that the two decimal points are lighted in the PAGER NO. display.
8	Momentarily press the TWO-WAY button.
9	Observe that the TWO-WAY lamp changes state (on/off).
10	Momentarily press the STORE button.
11	Release the PROGRAM button.
12	Perform the Status Check Procedure to see if the code is correctly programmed.

15. PROCEDURE TO INACTIVATE A PAGER CODE

STEP	PROCEDURE
1	Press and hold the PROGRAM button.
2	Using the keyset on the front panel, enter the two digits for the pager code that you want to make inactive.
3	Observe that the DIALED NO. display indicates the entered number.
4	Press the CHANGE NO. button and release it.
5	Observe that the two decimal points are lighted in the PAGER NO. display. This means that the next operation affects the pager number.
6	Momentarily press the INACTIVE button.
7	Observe that the INACTIVE lamp is lighted.
8	Momentarily press the STORE button.
9	Release the PROGRAM button.
10	Perform the Status Check Procedure to check that the number is inactive, and the system is properly programmed.

16. TO RE-INSTATE AN INACTIVATED PAGER CODE

STEP	PROCEDURE
1	Press and hold the PROGRAM button.
2	Observe that two decimal points appear in the DIALED NO. window.
3	Using the keyset, enter the two-digit code for the pager that you want to re-instate.
4	Observe that the DIALED NO. display indicates the correct code.
5	Observe that the INACTIVE lamp is lighted.
6	Momentarily press the CHANGE NO. button.
7	Observe that the two decimal points are lighted in the PAGER NO. display.
8	Momentarily press the INACTIVE button.
9	Observe that the INACTIVE lamp goes out.
10	Momentarily press the STORE button.
11	Release the PROGRAM button.
12	Perform the Status Check Procedure to see if the code is correctly programmed.

17. PROGRAMMING AN ALTERNATE PAGER CODE (UNI)

STEP	PROCEDURE
1	Determine the two-digit code for the pager that is being removed from service.
2	Press and hold the PROGRAM button.
3	Observe that the DIALED NO. display has two decimal points in the display.
	NOTE The decimal points indicate that the keyset is enabled, and that any number entered will affect the DIALED NO.
4	On the keyset, enter the two-digit code for the pager (step 1).
5	Check that the correct number is displayed in the DIALED NO. window.
6	Momentarily press the CHANGE NO. button.
7	Observe that the two decimal points have moved from the DIALED NO. display to the PAGER NO. display.
	NOTE The decimal points now indicate that any number entered on the keyset will affect the PAGER NO.
8	Determine the two-digit code for the substitute pager.
9	Enter the two-digit substitute pager code on the keyset.
10	Check that the correct number is displayed in the PAGER NO. window.
11	If the panel display is correct, momentarily press the STORE button.
	NOTE The conditions indicated will be stored, including INACTIVE and TWO-WAY.
12	Release the PROGRAM button.
13	Check the program as described in the Status Check Procedure.

18. TWO-WAY OPERATIONAL CHECKS

This section describes the additional post installation setup procedures and initial adjustments required for two-way operation. Perform all the preceding preoperational adjustments, level settings, and tests before proceeding with the two-way operational checks.

NOTE

When performing the Test Paging Procedure described in paragraph 10, make sure that the pager code dialed is programmed for one-way operation.

a. Receive Audio Sensitivity

Connect an oscilloscope to monitor the output of Schmitt trigger U6B (pin 4 on Two-Way Board) and, using a service monitor, transmit a signal to the base station with a 1 kHz tone at 1 kHz deviation. Adjust potentiometer R9 to just past the threshold where a square wave output is observed.

NOTE

In some systems it may be necessary to adjust R9 using an actual voice transmission from a paged radio instead of the service monitor to ensure VOR detection.

b. Jumper Placement Options

Jumper settings for the input and main terminal boards are the same as described in paragraph 9, except that JU1 is installed to provide two-way operation.

NOTE

Without a UNI, all pagers in the system are programmed for two-way (JU1 in) or one-way (JU1 out) operation.

c. Two-Way Board Jumper Options

(1) JU1 - Carrier/Voice Switching

Jumper JU1 is factory installed to provide VOR (Voice Operated Receive) and VOX (Voice Operated Transmit) switching. In systems wired for COR (Carrier Operated Relay) switching, jumper JU1 must be removed.

(2) JU2 - Allotment Time

With no jumper installed, the allotted time duration of the two-way conversation is approximately 60 seconds, since the high "Q3" output of U5 via resistor R24 appears at point A. This period may be extended to a maximum of three minutes or decreased to a minimum of 20 seconds. Twenty-second increments of allotment time are provided in this range by installing jumper JU2 from point A to any of the following points:

B - 20 seconds	H - 120 seconds
C - 40 seconds	J - 140 seconds
D - 80 seconds	K - 160 seconds
F - 100 seconds	L - 180 seconds

(3) JU3 - Squelch Tail Suppression

When the base station transmitter is turned off and the receiver switched on, the squelch circuit is activated and turns off the receiver audio circuits in the absence of a received carrier. Since the squelch circuit cannot respond immediately, an internally generated "rushing" noise will be heard through the radio speaker for a short duration before the receiver is quieted. This burst of noise is called a squelch tail and the length of time that it exists varies, depending on the type of base station and the response time of the internal squelch control circuit.

To prevent this squelch tail from being detected as received audio, the two-way board logic is programmed at the factory to provide a 0.6-second delay ("Q5" high applied to point A through R13) before the state decoder/generator switches from transmit (State 8) to monitor (State 9). This 0.6-second delay is obtained with JU3 deleted.

If a shorter or longer delay is required, JU3 can be field installed by connecting point A to points B (0.3 second), D (1.2 seconds), or E (2.4 seconds). The delay should be adjusted for the shortest time necessary to suppress detection of the squelch tail.

SUBSCRIBER OPERATION

1. GENERAL

This section describes the different procedures for paging a party. There are several procedures that can be used, depending upon the type of pager, the way the system is programmed, and the telephone used to initiate the page.

The page can be initiated from a normal telephone in the PABX system, or from an optional "priority" telephone. The telephones may be either dial-pulse or tone coded (DTMF) telephones, depending upon how the terminal is equipped.

In systems where tone-only pagers, tone-and-voice pagers, and two-way pagers (selective-call radios) are mixed, the operator must know which type pager the party is carrying. The most common type pagers encountered in a PABX paging system are one-way tone-and-voice pagers.

2. HOW TO PLACE A PAGE (One-way, tone-and-voice pagers)

STEP	PROCEDURE
1	Determine the two-digit pager code for the party you wish to contact.
2	Lift the telephone off-hook.
3	Dial the terminal access code. a. Line Level - Ring-back will be heard until the terminal answers the line, BUSY lamp on after a 3-second billing delay a "go-ahead" tone will be heard. b. Selector Level - BUSY lamp on, shortly after the terminal answers the line a "go-ahead" tone will be heard.
4	If you hear a "busy" tone, hang up and return to step 2. If you hear the "go-ahead" tone, proceed to the next step.
5	Dial the two-digit pager number.
6	Listen for the acknowledge (beeping) tone, indicating the page is being transmitted.
7	When the beeping tone stops, speak your message to the called party. You have about 15 seconds to talk. **NOTE** Your allotted time has expired when you hear the "busy" tone returned to the telephone (DCW only).
8	Hang up the telephone when you are finished talking or when the allotment time has expired.

3. PRIORITY TELEPHONE PAGING PROCEDURE

STEP	PROCEDURE
1	Determine the two-digit pager code for the party you wish to contact.
2	Lift the telephone off-hook. **NOTE** If the red "BUSY" indicator on the priority telephone is illuminated while the telephone handset in on-hook, then a normal "dialed-in" is in progress. Lifting the priority phone off-hook will interrupt any page in progress and return the invalid warble tone to the caller.
3	Listen for a "go-ahead" tone in the receiver.
4	Dial the two-digit pager number.
5	Listen for the acknowledge tone, indicating that the page is being transmitted.
6	When the beeping tone stops, speak your message to the called party.
7	Hang up the telephone when you are finished talking. **NOTE** There is no allotment time-out for priority calls.

4. TWO-WAY OPERATION

a. General

Placing a two-way page is the same as placing a one-way page up to the point when the acknowledge (beeping) tone indicates that the paging tones are being transmitted. When the beeping tone stops, a two-way conversation period exists and the Sending Party must make the initial contact by speaking into the telephone.

To eliminate confusion and to prevent inefficient use of air time, all users of the system should be familiar with conventional two-way radio operating procedures. In addition, all operators should be aware of the type of switching employed in the terminal to change from transmit mode to receive mode and the reverse. The two switching modes available are Carrier Operated Relay (COR) and Voice Operated Receive (VOR)/ Voice Operated Transmit (VOX).

NOTE

When the terminal is in the transmit mode, the Sending Party may speak and be heard by the Receiving Party. In the receive mode the opposite is true.

The two-way conversation period is limited by internal programming in the terminal. It is normally set for time-out after approximately one minute; however, different systems may vary from 20 seconds to three minutes. All users of the system should be aware of their allotment time.

A warning tone, similar to the go-ahead tone, will be heard approximately ten seconds prior to timeout. Ten seconds after the warning, tone, the call is terminated with no indication to either party, and the Sending Party should hang up the telephone.

NOTE

The Receiving Party will not hear the warning tone if speaking at the time the tone is generated.

To maintain a two-way conversation for the entire time allotted, each party must respond within five seconds; otherwise, the call will be terminated with no warning tone generated. To prevent premature timeout, using the word "over" at the end of each transmission will indicate to the other party that you are through speaking and a response is expected.

b. Cor Switching Mode

In a system using COR switching, the Receiving Party controls the conversation; i.e., whenever the radio's push-to-talk switch is depressed, the base station repeater detects a carrier, which operates a relay, causing the terminal to switch to the receive mode. This allows the Receiving Party to interrupt the Sending Party and the Sending Party should be aware that the voice message will not be transmitted whenever the Receiving Party is speaking.

c. VOX/VOR Switching Mode

In a system using VOX/VOR switching, if the Sending Party does not speak within five seconds after the tones are transmitted, the call will be terminated with no warning indication. Once the Sending Party speaks, however, the presence of transmit audio prevents the terminal from switching to the receive mode and the Sending Party maintains control of the system until the allotment timer times out or until a two-second period of silence (transmit) is detected. After two seconds of silence, the terminal switches to a monitor cycle.

In the monitor cycle, the terminal will respond to voice audio from either party and switch to the appropriate state (transmit or receive) depending on which party speaks first.

If the Receiving Party speaks, receive audio is detected and the terminal switches to the receive mode, allowing the Receiving Party to maintain control until the allotment timer times out, or until a two-second period of silence (receive) is detected. After two seconds of silence, the terminal returns to the monitor cycle.

If the Sending Party speaks, transmit audio is detected and the terminal switches back to the transmit mode, returning control to the Sending Party.

If neither party speaks, the terminal will stay in a monitor cycle for approximately five seconds, after which time the call will be terminated with no indication to either party.

THEORY OF OPERATION

1. INTRODUCTION

This section of the manual provides both a basic and a detailed functional description of the paging terminal and its components. Overall functions are discussed first in general terms followed by a detailed description of each printed circuit board used in the terminal. These detailed descriptions are intended to be used in conjunction with the logic and schematic diagrams. In addition, the appendices contain descriptions of basic logic circuits and a complete set of data sheets on each integrated circuit package used in the terminal.

The basic functions performed by the paging terminal are as follows:

a. Receive, via a telephone line, the subscriber number of the person being paged.

b. Convert the dialed code number into a series of paging tones.

c. Link the paging tones and associated voice message (tone and voice systems only) to a base station for transmission over the air.

2. BASIC FUNCTIONAL DESCRIPTION

A simplified composite block diagram of the terminal is shown in Figure 38. All four available input boards are shown; however, only one of the boards can be installed in the terminal. The standard terminal includes the dial pulse board for selector level connection. The DCK or DCW exchange adapters are leased items from the telephone company, whereas the NLN5114A Interface Kit (FCC Registered) is supplied with the terminal when either of the line level input boards are ordered.

a. Selector Level Input Boards

The selector level input boards contain the detection and response circuitry required to satisfy the relay closure conditions expected by the DCK/DCW telephone company exchange adapter. In addition, they provide the tone decoding and pulse detection circuitry necessary for conversion of the dialed input to BCD information, which is passed on to the UNI and/or main terminal board. The priority telephone input is also processed through these boards.

When a seize condition is detected or the priority phone is lifted off-hook, an acknowledge tone is returned to the caller, indicating that the pager code may be dialed. When the last digit is decoded, the caller will hear a beeping tone, as paging tones are being transmitted. When the beeping tone is finished, the two-way audio path is opened and the call allotment timer is started, providing approximately 14 seconds for the caller to complete his voice message.

NOTE

There is no allotment time-out for priority calls.

Figures 39 and 40 show the functional blocks for the dial pulse and tone input boards, respectively.

b. Line Level Input Boards

The line level input boards perform the same control signals as the selector level boards. They differ in that the interface with the PABX at the connector level via the Motorola NLN5114A Line Level Protection Circuit (FCC Registered). Telephone company exchange adapters are not required at the connector level. Figures 41 and 42 show the functional blocks for the dial pulse and tone input boards, respectively.

c. Main Terminal Board

The main terminal board circuitry includes the following:

- Control Logic
- Tone Generator-Synthesizer
- Transmitter Control
- Tone Timing
- Shared Channel Monitoring
- Emergency Page (optional)
- Automatic Station Identification (ASI) Circuits

BCD information and appropriate control signals are received from either the input board or the UNI to generate a two-tone page. The BCD information determines the tone A and tone B frequencies. The synthesizer circuitry can generate ten different tones from any standard tone group or combinations, as determined by the plug-in ROM's. The frequency of these tones cannot be changed, unless new ROM's are installed. Figure 43 is a simplified functional block diagram of the main terminal board. Figure 44 shows the audio control circuitry.

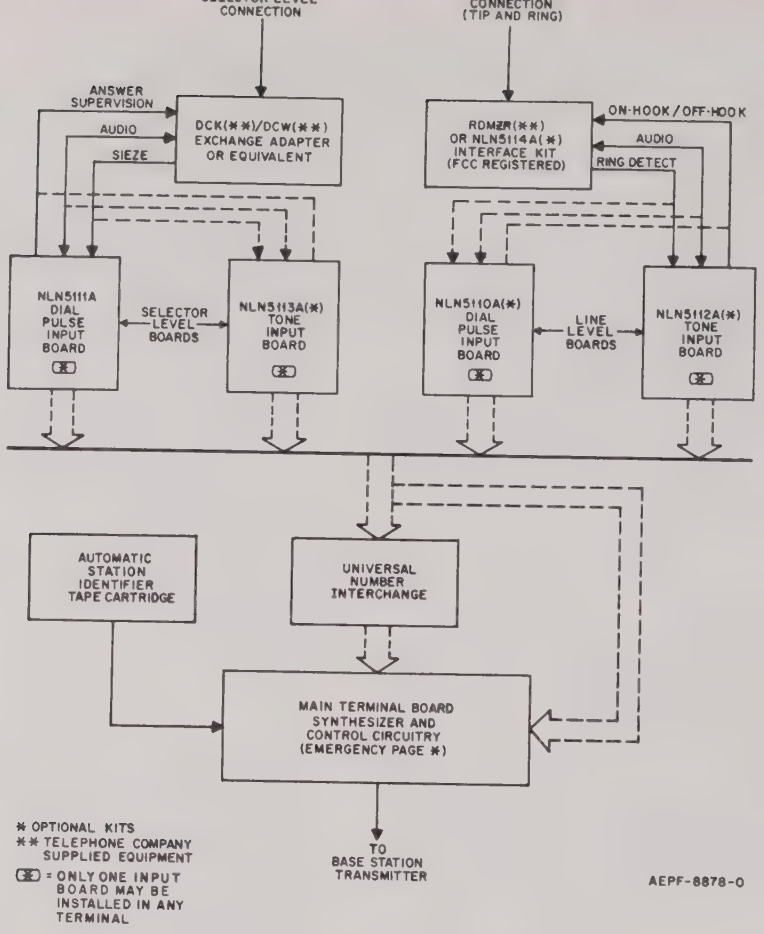


Figure 38. Simplified Terminal Block Diagram

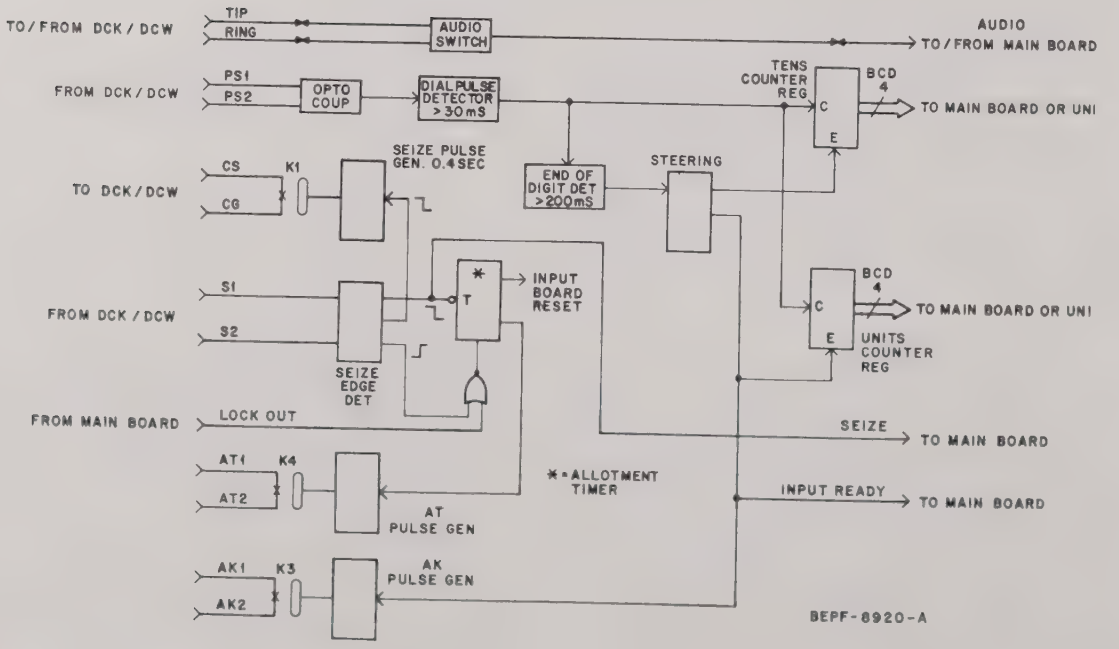


Figure 39. Dial Pulse Input Board (Selector Level) Block Diagram

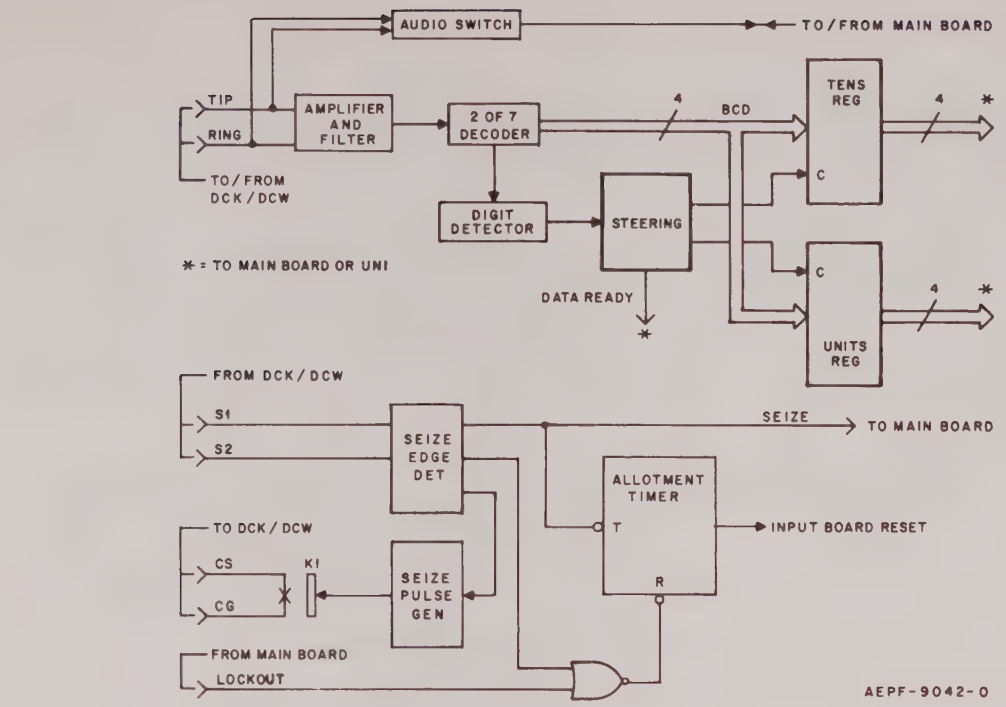


Figure 40.
Tone Input Board (Selector Level) Block Diagram

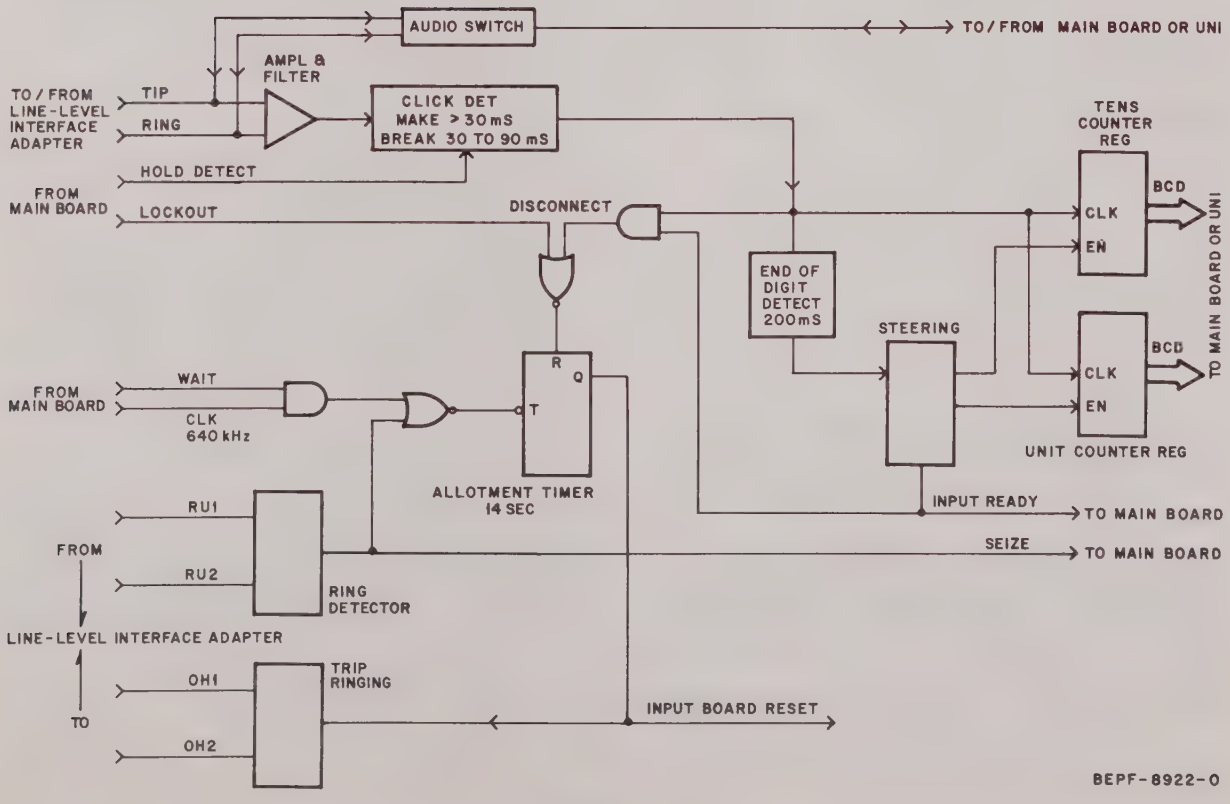


Figure 41.
Dial Pulse Input Board (Line Level) Block Diagram

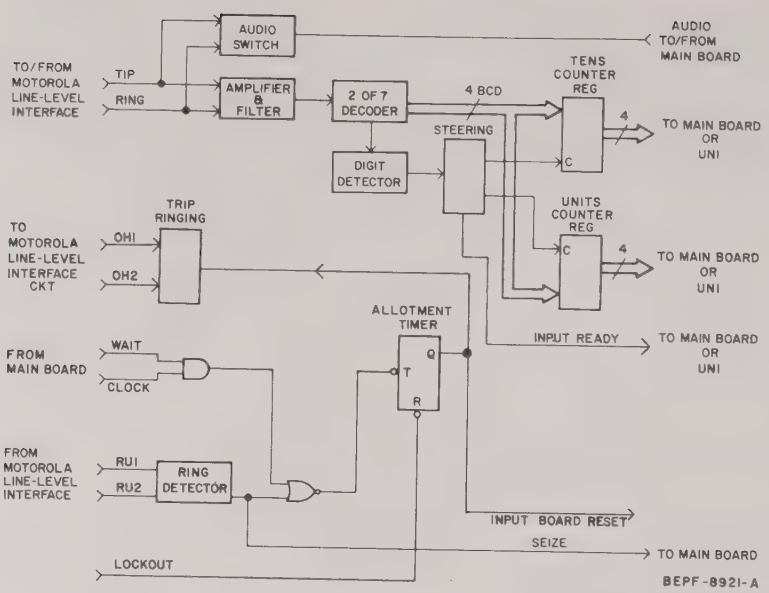


Figure 42. Tone Input Board (Line Level) Block Diagram

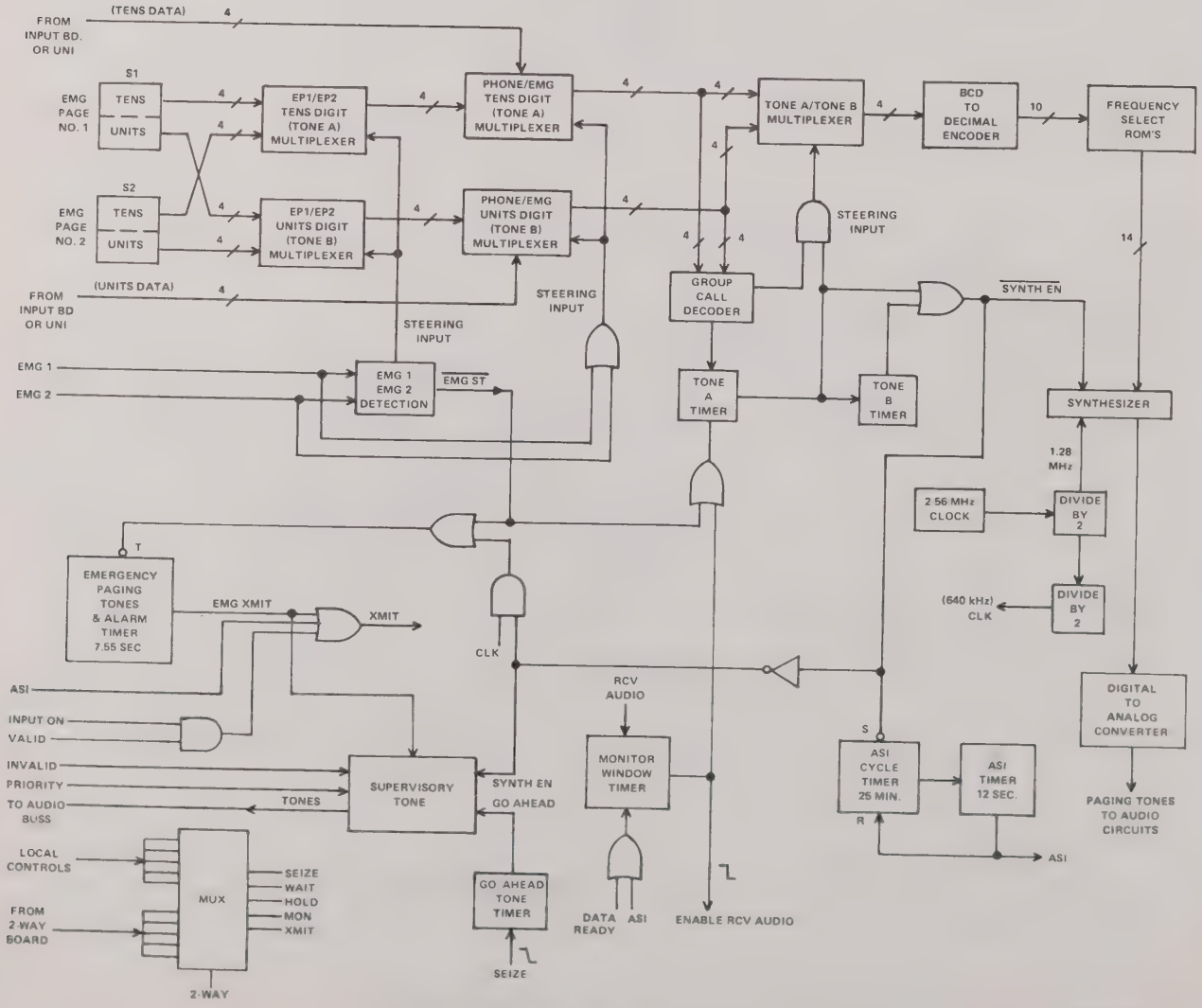


Figure 43. Main Terminal Board Block Diagram

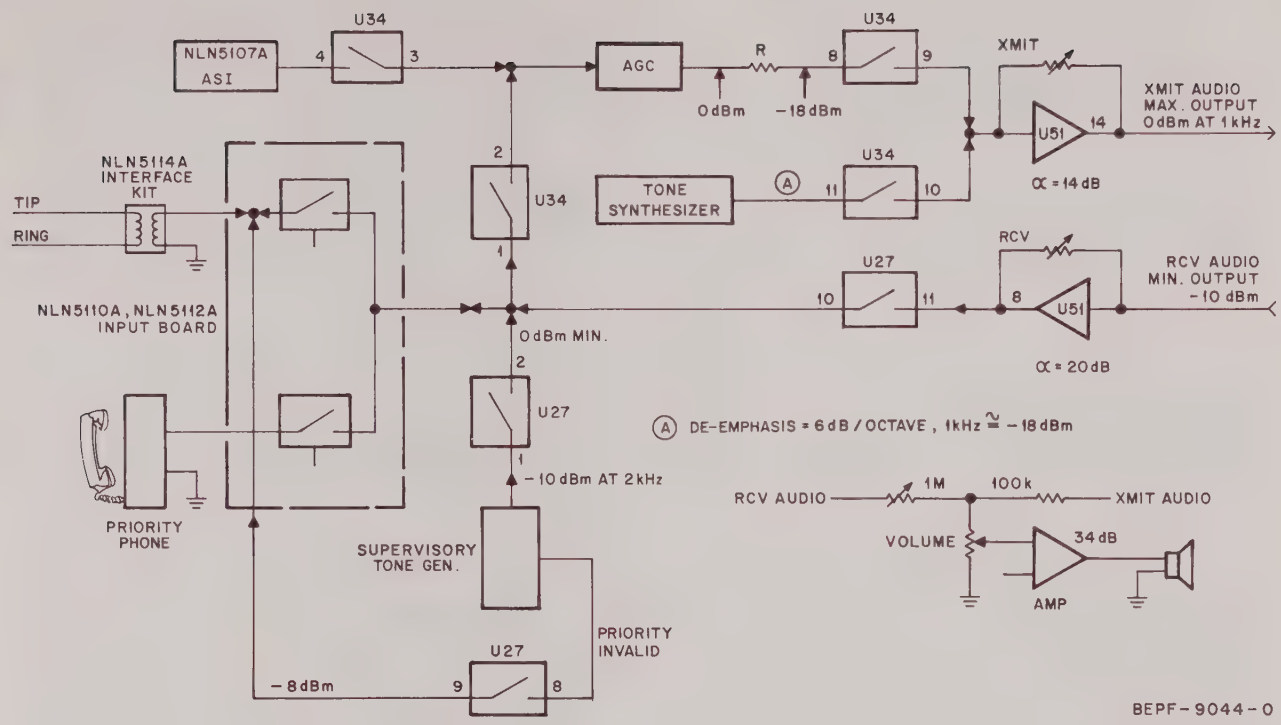


Figure 44. Simplified Audio Control Circuitry

d. Universal Number Interchange (UNI) Boards

The UNI circuitry is contained on two separate boards, namely, the UNI Primary Board and the UNI Display Board. Figure 45 represents a functional block diagram of these boards. All information from the input board must pass through the UNI before it reaches the main terminal board. The two-digit number from the input board is used to address an electrically alterable read-only memory (EAROM). The output of the EAROM for this address can be the same as the dialed pager code or any replacement number previously programmed via the front panel keyboard. The output of the UNI is then routed to the main terminal board.

e. Automatic Station Identifier (ASI)

The ASI is a standard eight-track tape cartridge player that responds to control signals from the main terminal board. It will start and play for approximately nine seconds 26 minutes after a page has been sent.

3. DETAILED CIRCUIT DESCRIPTION

a. NLN5111A Dial Pulse Input Board (Selector Level)

(Refer to schematic diagram 63E81015C58)

(1) In-Service Indication

When the calling party dials the assigned access (trunk) code, the DCK or DCW will return a busy signal unless relay K2 is energized to provide a contact closure across P8-4 (COS) and P8-5 (COG), indicating that the terminal system is available.

The system is normally available (K2 energized), however, there are three conditions that may cause the output of OR gate U8C to go low, de-energizing K2. These conditions are:

(a) If the priority phone is in use, the signal $\overline{\text{PRIORITY}}$ is inverted by gate U15C and applied as a high at pin 9 of U8C.

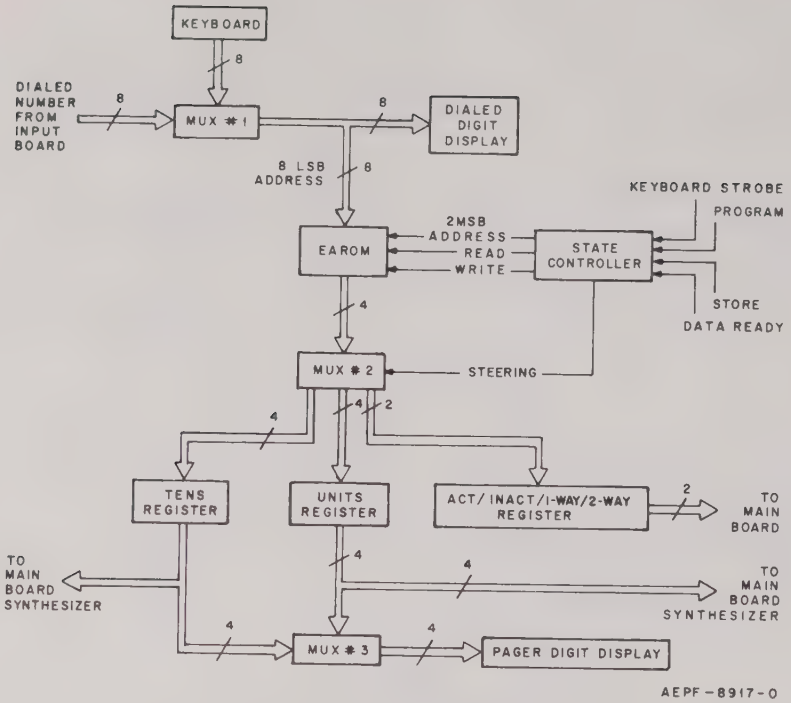


Figure 45. UNI Block Diagram

(b) If a lockout condition exists (emergency page in process, UNI PROGRAM button depressed, etc.), the signal $\overline{L.O.}$ (P7-2 and J2-14) is inverted by gate U22A and applied as a high at pin 8 of U8C.

(c) Whenever power is applied to the terminal, the power on reset ($\overline{RST}$) signal is generated on the maintterminal board to insure that all the logic is initialized in the proper state. During this reset period, the $\overline{RST}$ signal (J2-12) is inverted by gate U22A and applied as a high at pin 8 of U8C.

If the terminal is available, a relay closure in the DCK or DCW connects S1 (P8-6) to S2 (P8-10). This closure will exist for the entire period that the telephone is in contact.

(2) Seize Detection

With S1 low, transistor Q6 turns on, triggering one-shot U5A causing its "Q" output to go high for approximately 500 milliseconds. This high signal (SEIZE) energizes relay K1 and the closure across P8-2 (CS) and P8-5 (CG) provides the equipment ready (seize acknowledge) response required by the DCK or DCW to establish the two-way audio path between the telephone company equipment and the paging terminal.

The seizure level (S1 low) is also applied as a high on pin 2 of gate U8A in preparation for hang-up detection.

The 500-millisecond SEIZE pulse starts allotment timer U5B and at the same time is sent to the main terminal board via J2-9. When the trailing edge of the SEIZE pulse is detected on the main terminal board, a 1500 Hz "go-ahead" tone is returned via J2-3 through analog switch U14B to the caller. This alerts the caller that the pager code digits may be dialed.

NOTE

The BUSY indicator on the front panel will light and remain lit as long as the allotment timer is enabled.

(3) Dial Pulse Detection

When the pager code is dialed, each digit is converted to a series of pulses by the telephone company equipment and presented to the input board at P8-9 (PS1) and P8-11 (PS2). Since the priority phone is not in use, analog switch U14C will be closed to pass the pulses from optical isolator U19, through inverter U12, to start timer U17A. The serial pulses must be separated by more than 30 milliseconds in order to be decoded, since the time constant for U17A is approximately 27 milliseconds.

The serial pulse output from U17A is sent through the data pulse line logic (U2A, U3C, and U3B) and applied to the clock inputs of counters U10A and U10B. The pulses are also applied to the input of the inter-digit timer (U18A). The "Q" output of U18A will remain high for approximately 200 milliseconds, thereby requiring a 200-millisecond separation between the tens and units digits. When the inter-digit timer times out, the low from pin 5 is inverted to a high that clocks steering flip-flop U9B.

The output of U9B enables the units counter in preparation for the second dialed digit and at the same time places a high on the "D" input of data ready flip-flop U9A. When the second pager code digit is processed and the inter-digit timer times out, a clock pulse is applied to U9A and the DATA READY signal is sent to the main board via J2-15.

(4) Data Ready Condition

The main terminal board returns a WAIT signal to the input board via J2-7 to restart and hold the allotment timer. During the WAIT period, an audio path is opened and the caller may hear any one of the following:

(a) Steady Tone (1500 Hz)

This tone indicates that a station identification (ASI) is being transmitted. The tone will terminate when the identification is completed and if the channel is not in use, after a 2.5-second monitor cycle, an acknowledge signal (series of short beeps) will be heard, indicating that the pager tones are being transmitted. When the beeping stops, the WAIT signal is removed and the caller has approximately 14 seconds to complete his voice message.

(b) Conversation

Upon receipt of DATA READY, the main terminal board initiates a monitor cycle to determine if the radio channel is in use. If the channel is busy, the voice audio will be heard and the acknowledgement tones (beeps) will not be returned until the channel is clear for approximately 2.5 seconds.

(c) Interrupted Tone (1500 Hz)

This is the acknowledgement tone that sounds like a series of beeps. It is returned to the caller after the monitor cycle (approximately 2.5 seconds) and indicates that the pager tones are being transmitted. When the beeping stops, the WAIT signal ends and the voice allotment timer is released. The voice message will now be accepted.

(d) Warbling Tone (1000/500 Hz)

If an inactive pager code is dialed, (systems with UNI only) an invalid warbling tone will be returned, indicating that the page cannot be processed and the caller should hang up.

The call may be interrupted at any time by a four-second warbling tone. This indicates that a priority call has been initiated and the selector level call has been pre-empted. The caller should hang up and try later.

(e) No Response

An emergency page will immediately dump any calls in process with no audio indication to the caller. If no tones are returned to the caller within 5 seconds of completing dialing, he should hang up and try later.

(5) Call Termination

If the voice message exceeds the allotted 14-second period, the allotment timer will time out, turning off the busy indicator on the front panel and resetting the input board in preparation for subsequent pages.

If the caller terminates the call before the alloted voice message interval, the seizure (S1) level goes high. This unseized condition is detected and used to trigger one-shot U18B, which in turn, resets the allotment timer and conditions the board to receive subsequent pages.

NOTE

With the DCK arrangement, if the caller does not hang up the seizure level will remain low preventing access to the terminal even though the BUSY indicator is turned off.

(6) DCW Acknowledge and Allotment Closures

When DATA READY is generated, U1B is triggered and relay K3 is energized for approximately 500 milliseconds to provide the AK1 (P8-3) and AK2 (P8-4) closure. This signal establishes the audio path through the DCW after the digits have been entered. Once the audio path exists, no more digits can be accepted.

If the call allotment timer (U5B) times out before the caller hangs up, the timer's negative going edge triggers one-shot U1A, energizing relay K4 for approximately 500 milliseconds. This relay closure across AT1 (P8-1) and AT2 (P8-2) causes the DCW circuitry to drop the call and switch to an alternate port, thus preventing the caller from tying up the terminal.

(7) Priority Telephone

When the priority phone is lifted off-hook, a closure occurs across TP (P7-5) and RP (P7-6), turning on current bias transistor Q5. This supplies a ten-milliampere current loop to the priority phone. When Q5 conducts, Q4 and Q3 are turned on and the signal $\overline{\text{PRIORITY}}$ is generated. This signal is inverted to PRIORITY (U4A), and with these two signals present, the following events occur:

(a) PRIORITY is sent to the main terminal board through J2-5 via gate U15C.

(b) Analog switch U14B opens, breaking the primary audio path between the main terminal board and the selector level telephone.

(c) Analog switch U14A closes, connecting the main terminal board audio to the priority phone.

(d) A four-second warbling tone is returned to the selector level phone TIP (P8-14) and RING (P8-13) via J2-4 (INVALID AUDIO) indicating that the call is being dumped.

(e) Analog switch U14C opens, disabling the digit input from the DCK or DCW arrangement.

(f) The board reset flip-flop (U18B) is triggered through the seize condition detection circuitry, and the selector level call is dumped.

(g) The "in service indication" relay closure (K2) is removed so that a busy signal will be returned to any caller trying to access the terminal while the priority phone is off-hook.

(h) Allotment time-out is defeated by a constant low on the output of U16C which enables retriggering of the allotment timer by the clock pulses via U16B and U16A.

(i) The BUSY indicator on the front panel is turned on.

(j) A "go-ahead" tone is returned to the priority phone.

When the pager code digits are dialed, the serial pulses are passed from optical isolator U20, through inverter U12, to start timer U17A and the page is processed in the same manner as from the selector level phone. The digit bridging circuit (Q3, Q4, and Q5) bridges or filters the pulses so that the $\overline{\text{PRIORITY}}$ signal is not interrupted by dialing.

When the priority call is terminated the allotment timer will time out resetting the board in preparation for subsequent calls. Also, the "in service" condition will be restored.

b. NLN5110A Dial Pulse Input Board (Line Level)

(Refer to schematic diagram 63E81015C58)

The line level input board is connected to the telephone company equipment through the NLN5114A Line Level Protection Circuit described in instruction manual 68P81102C90. This protective interface circuitry isolates the terminal from the telephone network and provides the relay closures and control signals required for proper terminal operation.

(1) Seizure

When the terminal number is dialed (in the same manner as dialing a telephone extension number) the ringing is detected by the interface circuit and a relay closure connects RU1 (P8-6) to RU2 (P8-10). RU1 low turns on transistor Q6, triggering one-shot U5A causing its "Q" output to go high for approximately 3.5 seconds. Allotment timer U5B is turned on and its output, via U15D and U4C, turns on transistors Q8 and Q9.

Q8 "on" lights the BUSY indicator on the front panel and Q9 "on" provides a "service request" closure across OH1 (P8-7) and OH2 (P8-12). The service request seizes the line and, after a two-second minimum billing delay, provides a two-way audio path via TIP (P8-14) and RING (P8-13).

When U5A times out, the trailing edge of the 3.5-second SEIZE pulse is detected on the main terminal board (J2-9) and a 1500 Hz "go-ahead" tone is returned, via J2-3 through analog switch U14B to the caller. This alerts the caller that the pager code digits may be dialed.

(2) Digit Detection

When the pager code digits are dialed, the noise signals (clicks) generated by the breaking and making of the telephone dial contacts are applied to amplifier U21A. The gain of this stage is determined by the proper selection of feedback resistor R9, R10, R11, or R12 as explained in the Operating Procedures section of this manual. Figure 46A shows the typical noise signals received from the telephone dial contacts.

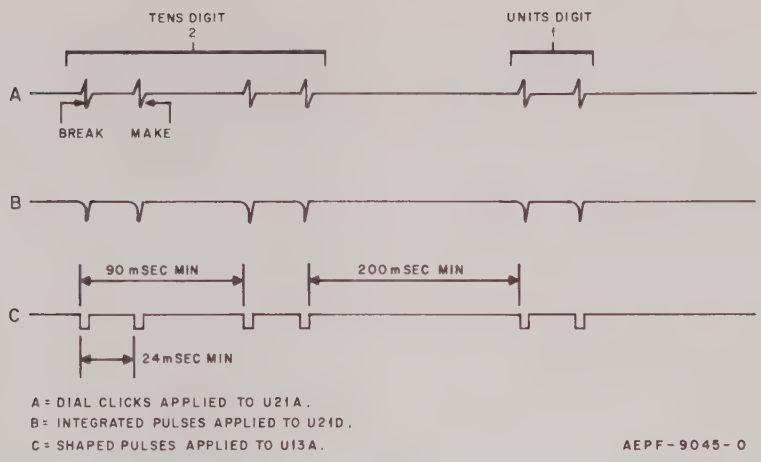


Figure 46.
Typical Break and Make Signal Waveforms

The pulses are processed through a low-pass filter (U21B) where any voice information is attenuated so that if the caller is speaking while dialing, it will not cause any interference. After processing through high-pass filter U21C, the signals are integrated and rectified before being applied to amplifier U21D. Figure 46B shows the integrated waveforms at the input of U21D and Figure 46C shows the output waveforms after shaping through U7B and U7C.

The first "break" pulse triggers U13A for approximately 24 milliseconds and its "Q" output, via U7D, triggers U13B for approximately 90 milliseconds. The "Q" output from U13B, via U7E, enables flip-flop U2B. The first "make" pulse must arrive after U13A times out, but before U13B times out, otherwise the pager code digits will not be decoded properly. When U13A times out, its "Q" output will go low with no effect on the circuit. When the second edge pulse (make) triggers U13A again, its "Q" output will clock the data pulse through U2B to the clock inputs of counters U10A and U10B. At the same time, the "$\overline{Q}$" output of U2B going high shortens the time-out period of U13B in preparation for subsequent break and make pulses.

When the remainder of the edge pulses for the tens digit are counted, the 200 millisecond interdigit gap will allow the U18A to time out clocking steering flip-flop U9B which enables the units digit counter (U10B).

Once the digits are decoded, DATA READY is sent to the main terminal board and the page is processed in the same manner as described for the selector level board in the preceding paragraph. The only differences are that HOLD DETECT from the main terminal board via JU2-8 prevents any additional digits from being detected and when the priority telephone is lifted off-hook, the signal $\overline{\text{PRIORITY}}$ holds U13A reset to prevent digit detection.

When the allotment timer times out, the BUSY indicator is turned off and the "service request" closure is removed.

(3) Hang-Up Detection

When the call is terminated by hanging up the phone, the "click" is detected and clocks flip-flop U6A. Since DATA READY is high, the "Q" output from U6A triggers U18B, which resets the allotment timer and initiates the board for receiving the next page.

c. NLN5113A Tone Input Board (Selector Level)

(Refer to schematic diagram 68P81015C59)

(1) Seizure

When the access code is dialed and the terminal is available, the DCK or DCW provides a closure across P8-6 (S1) and P8-10 (S2), turning on transistor Q17 which triggers timer U9B. The output of U9B will go high for approximately 500 milliseconds, energizing relay K1 to provide the equipment ready closure across P8-2 (CS) and P8-5 (CG). This establishes the two-way audio path between the telephone company equipment and the paging terminal.

NOTE

When the terminal is connected via the DCW, option "R" is required (or the ER1 and ER2 terminals must be shorted), and the K1 relay closure is connected to AK1/AK2 to establish the voice path.

The 500 millisecond SEIZE pulse starts allotment timer U9A and at the same time is sent to the main terminal board via J2-20. When the trailing edge of the SEIZE pulse is detected on the main terminal board, a 1500 Hz "go-ahead"

tone is returned through analog switch U3B to the caller. This alerts the caller that the paging digits may be dialed.

NOTE

The BUSY indicator on the front panel will light and remain lit as long as the allotment timer is enabled.

(2) Tone Decoding

Each pager digit is represented by a pair of audio tones simultaneously applied to the dual-tone, multiple-frequency (DTMF) decoding circuit. The tones enter the input board through the TIP (P8-14) and RING (P8-13) contacts and are routed through analog switch U3B to the decoder. The pager digit/tone pair relationship is as follows:

DIGIT	TONE FREQUENCIES (Hz)
1	697/1209
2	697/1336
3	697/1477
4	770/1209
5	770/1336
6	770/1477
7	852/1209
8	852/1336
9	852/1477
0	941/1336

The four low tones are attenuated by the high pass filter and the three high tones are attenuated by the low pass filter before processing through the log compression and comparator circuitry.

Assuming that pager code 24 is dialed, the tens digit (2) will produce an output from active filters U18 (697 Hz) and U23 (1336 Hz). After being integrated, provided that the tone time period lasts for a minimum of 20 milliseconds, a low will be applied at pins 1 and 6 of decoder U5, and a BCD representation of the tens digit (0010) will appear at the data outputs.

The strobe output from U5 is controlled by the 4000 Hz oscillator (U6B). For a strobe output to occur, the input lines (pins 1 through 7) must remain stable for 80 clock pulses. With a 4000 Hz clock rate, the strobe pulse will be generated 20 milliseconds after the digit is detected. The strobe pulse occurs only once for each valid digit.

The strobe is used to clock flip-flops U11B and U11A. Since the tens digit is being processed, the "Q" output of U11B will go high, transferring the BCD information through U12 to the main terminal board. The strobe applied to U11A has no effect on the circuit since its "Q" output was already low. However, the "Q" output from U11B is applied to the "D" input of U11A in preparation for clocking the units digit.

When a strobe pulse is generated 20 milliseconds after detecting the units digit, the "Q" output of U11A will go high, transferring the BCD information through U13 to the main terminal board. At the same time, the DATA READY signal is generated by U7B and is sent to the main terminal board via J2-15.

(3) Data Ready Condition

The main terminal board returns a WAIT signal to the input board via J2-7 to hold the allotment timer and provide an additional 14 seconds for completion of the voice message. During the WAIT period, an audio path is opened and the caller (after a 2.5-second monitor cycle) should hear an acknowledgement tone that sounds like a series of beeps. This indicates that the paging tones are being transmitted, and when the beeping stops, the voice message will be accepted.

If the acknowledge tone is not returned, one of the following conditions exists:

(a) The station identification is being transmitted.

(b) The base station is busy.

(c) An inactive pager code was dialed.

(d) A priority call has been initiated.

(e) An emergency page is in process.

The terminal responses for these conditions are described in the dial pulse input board paragraph.

(4) Call Termination

If the voice message exceeds the allotted 14-second period, the allotment timer will time out, turning off the busy indicator on the front panel and resetting the input board in preparation for subsequent pages.

If the caller terminates the call before the allotted voice message interval, the seizure (S1) level goes high. This unseized condition is detected and used to trigger one-shot U6A, which, in turn, resets the allotment timer and conditions the board to receive subsequent pages.

(5) Priority Telephone

When the priority phone is lifted off-hook, a closure occurs across TP (P7-5) and RP (P7-6), turning on bias transistor Q7. This supplies a 20-milliampere current loop to the priority phone, regulated by transistor Q1. When Q7 conducts, Q3 and Q2 are turned on and the signal PRIORITY is generated. This signal is inverted to PRIORITY through U8A, and with these two signals present, the following events occur:

(a) PRIORITY is sent to the main terminal board through J2-5 via gate U4B.

(b) Analog switch U3B opens, breaking the primary audio path between the main terminal board and the selector level telephone.

(c) Analog switch U3C closes, connecting the main terminal board audio to the priority phone.

(d) A four-second warbling tone is returned to the selector level phone via J2-4, indicating that the call is being dumped.

(e) The board reset flip-flop (U6A) is triggered and the selector level call is dumped.

(f) Relay K2 is de-energized so that a busy signal will be returned to any caller trying to access the terminal while the priority phone is off hook.

(g) Allotment time-out is defeated by a constant low on the output of U10C which enables retriggering of the allotment timer by the clock pulses via U10A and U16D.

(h) The BUSY indicator on the front panel is turned on.

(i) A "go-ahead" tone is returned to the priority phone.

When the pager code is dialed, the tones are routed through analog switch U3C to the DTMF decoding circuitry; otherwise the call is processed in the same manner as a selector level call.

When the priority call is terminated, the allotment timer will time out, resetting the board in preparation for any subsequent calls. Also, the "in service" condition will be restored.

d. NLN5112A Tone Input Board (Line Level)

(Refer to schematic diagram 63E81015C59)

There are only two functional differences between the line level input board and the selector level input board. One difference is the method by which the line is seized and the other is the method used to detect a terminated call.

(1) Seizure

When the terminal extension number is dialed, the ringing is detected by the interface circuit and a relay closure connects P8-6 (RU1) to P8-10 (RU2).

NOTE

The NLN5114A Line Level Protection Circuit is described in instruction manual 68P81102C90, which is supplied with the terminal when a line level input board is ordered.

RU1 going low turns on transistor Q17, triggering one-shot U9B causing its "Q" output to go high for approximately 3.5 seconds. Allotment timer U9A is turned on and its output, via U16B and U8B, turns on transistors Q6 and Q8.

Q6 "on" lights the BUSY indicator on the front panel and Q9 "on" provides a "service request" closure across P8-7 (OH1) and P8-12 (OH2). The service request seizes the line and, after a two-second minimum billing delay, provides a two-way audio path via P8-14 (TIP) and P8-13 (RING).

When U9B times out, the trailing edge of the 3.5-second SEIZE pulse is detected on the main terminal board (J2-9) and a 1500 Hz "go-ahead" tone is returned via J2-3 through analog switch U3B to the caller. This alerts the caller that the pager code digits may be dialed.

(2) Hang-Up Detection

When the caller terminates the call by "hanging-up" the phone, a spiked signal is felt at the input of the hang-up detection circuit. This signal is integrated by resistor R15 and capacitor C11 and after 60 milliseconds triggers comparator U1C. The U1C output, via U14B, is used to clock flip-flop U7A which has been enabled by the DATA READY signal. The "Q" output of U7A, via U14A, triggers U6A which in turn resets the allotment timer, initializing the board for the next page.

e. NLN5115A UNI Primary Board

(Refer to schematic diagram 63E81015C43)

The UNI primary board provides a straight through control signal and audio path between the input board and the main terminal board, and accepts BCD information from either the input board or the UNI display board. The input data (dialed number) is processed, depending on the existing terminal status conditions and/or the keyboard commands presented via the display board. There are two basic UNI operational modes, namely Run (on-line) and Program (off-line).

In the Run mode, the dialed number is used as an address for the EAROM, and the pager code stored in that location along with its status (active/inactive; one-way/two-way) information is passed to the main terminal board.

The Program mode is initiated by depressing and holding the PROGRAM button on the front panel. If the terminal is not busy, $\overline{\text{LOCKOUT}}$ is generated to prevent telephone access of the terminal. In this off-line mode, the keyboard is enabled so that:

- Pager status may be checked.
- An alternate pager code may be programmed.
- A pager code may be inactivated or reinstated.

(1) Memory Organization and Control

The ER3401 EAROM (U12) memory matrix is organized into 1024 four-bit words with each word individually accessible by a ten-bit word address.

Each pager code along with its status information (active/inactive and one-way/two-way) consists of ten information bits, thereby requiring three separate four-bit word storage locations. As a result, for 100 pager numbers (00 through 99), there are 300 addresses and three successive "reads" are required to retrieve each pager number and status. Table 23 shows the 300 memory storage locations used and illustrates the three specific addresses used to retrieve the data associated with pager code 46.

The addressing scheme uses the actual dialed pager number applied to the A0 through A7 address lines as a constant partial address for each of the three words. The A8 and A9 bits are incremented as a counter to sequentially address words 1, 2, and 3. For example:

(a) The address for word number 1 (Status) of pager code 46 would be:

A9	A8
2^9	2^8
0	1
256	

+

A7	A6	A5	A4
2^7	2^6	2^5	2^4
0	1	0	0
64			

+

A3	A2	A1	A0
2^3	2^2	2^1	2^0
0	1	1	0
4 + 2			

= 326

(b) The address for word number 2 (Tens) of pager code 46 would be:

A9	A8
2^9	2^8
1	0
512	

+

A7	A6	A5	A4
2^7	2^6	2^5	2^4
0	1	0	0
64			

+

A3	A2	A1	A0
2^3	2^2	2^1	2^0
0	1	1	0
4 + 2			

= 582

(c) The address for word number 3 (Units) of pager code 46 would be:

A9	A8
2^9	2^8
1	1
512 + 256	

+

A7	A6	A5	A4
2^7	2^6	2^5	2^4
0	1	0	0
64			

+

A3	A2	A1	A0
2^3	2^2	2^1	2^0
0	1	1	0
4 + 2			

= 838

The word address for any valid pager code can be determined using the memory address matrix shown in Table 23.

Initially, the UNI is factory programmed for "straight-through" operation with one-way and active status. This means that the address locations for pager code 46, for example, will contain the following information:

WORD 1			
2^3	2^2	2^1	2^0
X	X	0	1

NOT USED

ONE-WAY

ACTIVE

WORD 2			
2^3	2^2	2^1	2^0
0	1	0	0

4

WORD 3			
2^3	2^2	2^1	2^0
0	1	1	0

6

Table 23. Memory Address Matrix

	TENS DIGIT	UNITS DIGIT									
		0	1	2	3	4	5	6	7	8	9
STATUS WORD ADDRESS (A9 = 0; A8 = 1)	0	256	257	258	259	260	261	262	263	264	265
	1	272	273	274	275	276	277	278	279	280	281
	2	288	289	290	291	292	293	294	295	296	297
	3	304	305	306	307	308	309	310	311	312	313
	4	320	321	322	323	324	325	326	327	328	329
	5	336	337	338	339	340	341	342	343	344	345
	6	352	353	354	355	356	357	358	359	360	361
	7	368	369	370	371	372	373	374	375	376	377
	8	384	385	386	387	388	389	390	391	392	393
	9	400	401	402	403	404	405	406	407	408	409
TENS WORD ADDRESS (A9 = 1; A8 = 0)	0	512	513	514	515	516	517	518	519	520	521
	1	528	529	530	531	532	533	534	535	536	537
	2	544	545	546	547	548	549	550	551	552	553
	3	560	561	562	563	564	565	566	567	568	569
	4	576	577	578	579	580	581	582	583	584	585
	5	592	593	594	595	596	597	598	599	600	601
	6	608	609	610	611	612	613	614	615	616	617
	7	624	625	626	627	628	629	630	631	632	633
	8	640	641	642	643	644	645	646	647	648	649
	9	656	657	658	659	660	661	662	663	664	665
UNITS WORD ADDRESS (A9 = 1; A8 = 1)	0	768	769	770	771	772	773	774	775	776	777
	1	784	785	786	787	788	789	790	791	792	793
	2	800	801	802	803	804	805	806	807	808	809
	3	816	817	818	819	820	821	822	823	824	825
	4	832	833	834	835	836	837	838	839	840	841
	5	848	849	850	851	852	853	854	855	856	857
	6	864	865	866	867	868	869	870	871	872	873
	7	880	881	882	883	884	885	886	887	888	889
	8	896	897	898	899	900	901	902	903	904	905
	9	912	913	914	915	916	917	918	919	920	921

(2) Control State Decoding and Timing

The timing and sequencing of the erase, write, and read operations is determined by the control state decoder/generator logic in conjunction with the clock pulses developed through counters U31 and U37. A 20 kHz clock pulse from the "Q5" output of U31 (640 kHz ÷ 32) is applied to the "C" inputs of flip-flops U24A, U35B, U35A, U29B, and U29A producing a binary output which is decoded as a state signal by decoders U23, U28, and U34.

State signals are generated in a sequential loop, i.e., the decoded state signal is used to condition the inputs of the J-K flip-flops such that the next clock pulse will cause the state signal for the following operation to be decoded. For example, when State 3 (Read Status) is decoded, the "Q" outputs of U29A (2^0) and U29B (2^1) are high producing a high "Q3" output from U23. This high via gates U21A and U30A, is fed back to the "J" inputs of U35B (2^3) and U24A (2^4) and, with the next clock pulse, State 27 will be decoded (2^0 set = 1, 2^1 set = 2, 2^3 set = 8, 2^4 set = 16). Table 24 shows the state generation sequence and the operation associated with each state.

In addition, the state decoder logic produces the chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and mode control input (C0 and C1) signals as well as the most significant bits of the memory word addresses (A8 and A9). The wait time periods T1 (12.8 milliseconds) and T2 (1.6 milliseconds) are produced at the "Q7" and "Q4" outputs of counter U37, respectively. Figure 47 shows the master control state sequencing associated with the various command signals and Figure 48 shows the timing relationship of the memory control input signals.

(3) On-Line Operation

The BCD information from the input board is applied to the "Y" inputs of multiplexers U6 (tens data) and U7 (units data) and gated through to the "Z" outputs because the "B" control inputs are high due to the RUN signal being present.

The "Z" output data from the tens digit multiplexer (U6) is applied to the "X" inputs of the dialed number multiplexer (U5) and to the A4 through A7 address lines of EAROM U12. The "Z" output data from the units digit multiplexer (U7) is applied to the "Y" inputs of U5 and to the A0 through A3 address lines of U12.

Counter U31 is clocked by the 640 kHz signal from the main terminal board via J2A-6 and the "Q6" output (10 kHz) is applied to the "A" and "B" control inputs of U5 to alternately present the tens and units data to the UNI display board for the DIALED NO. display.

(a) Control State 0 (Quiescent)

When the UNI is idle, State 0 (Quiescent) exists and the "Q0" output of decoder U23 is high, priming gates U25A and U25B. When DATA READY is received, flip-flop U24B is clocked and its "Q" output (via U20A) enables gate U25B. The high from U25B (via U36A, U30C, and U30A) conditions the J-K flip-flops for decoding State 19 on the next clock pulse.

(b) Control State 19 (Start Read)

When State 19 is decoded, the "Q3" output of decoder U28 goes high. This high is applied through gate U26C to the "K" input of U24A in preparation for decoding State 3 on the next clock pulse.

(c) Control State 3 (Read Status Word)

When State 3 is decoded, flip-flops U24A, U35B, and U35A are reset, selecting memory address word number 1 (A9 = 0, A8 = 1) and a low is applied to the "C0" mode control input of U12. The C1 mode control input to U12 is always low unless Control State 4, 28, or 20 is decoded. Therefore, U12 is conditioned to read word number 1 (Status).

In the Read mode, data is read from memory during the chip enable ($\overline{CE}$) pulse which requires three simultaneous low inputs to gate U26B. Pin 4 of U26B goes low on the negative half cycle of the 20 kHz clock pulse. Pin 3 will always be low, unless an illegal state (8 through 15 or 24) is decoded. Pin 5 will be low unless State 0 or any one of the wait states (5, 6, 21, 22, 29, or 30) is decoded.

With A9 = 0, A8 = 1, and C0 = 0, the outputs of gates U13A and U13B will be low and with the "A" and "B" control inputs to analog multiplexers U8 and U9 low, the "X0" and "Y0" outputs are selected. The 2^0 (active/inactive) and 2^1 (one-way/two-way) bits of the status word are sent to the display board via P4-6 and P3-15, respectively. The 2^2 and 2^3 bits of the status word are not used.

When State 3 is decoded, the "Q3" output of decoder U28 goes high. This high is applied through gates U21A and U30A to the "J" inputs of U24A and U35B. Since flip-flops U29A and U29B are already set, the next clock pulse will decode State 27.

Table 24. Memory Cycle Control State

STATE SIGNAL	OPERATION	A9	A8	C0	C1	CE
0	QUIESCENT	0	1	0	0	1
	(NEXT STATE SIGNAL = 4 or 19)					
4	START STATUS ERASE	0	1	1	1	0
5	WAIT FOR TIME 1	0	1	1	0	1
	(T1 = 12.8 milliseconds)					
1	END STATUS ERASE	0	1	0	0	0
7	START STATUS WRITE	0	1	1	0	0
6	WAIT FOR TIME 2	0	1	1	0	0
	(T2 = 1.6 milliseconds)					
2	END STATUS WRITE	0	1	0	0	0
28	START TENS ERASE	1	0	1	1	0
29	WAIT FOR TIME 1	1	0	1	0	1
	(T1 = 12.8 milliseconds)					
25	END TENS ERASE	1	0	0	0	0
31	START TENS WRITE	1	0	1	0	0
30	WAIT FOR TIME 2	1	0	1	0	1
	(T2 = 1.6 milliseconds)					
26	END TENS WRITE	1	0	0	0	0
20	START UNITS ERASE	1	1	1	1	0
21	WAIT FOR TIME 1	1	1	1	0	1
	(T1 = 12.8 milliseconds)					
17	END UNITS ERASE	1	1	0	0	0
23	START UNITS WRITE	1	1	1	0	0
22	WAIT FOR TIME 2	1	1	1	0	1
	(T2 = 1.6 milliseconds)					
18	END UNITS WRITE	1	1	0	0	0
19	START READ	1	1	0	0	0
3	READ STATUS	0	1	0	0	0
27	READ TENS	1	0	0	0	0
16	READ UNITS	1	1	0	0	0
0	QUIESCENT	0	1	0	0	1

8→15	ILLEGAL STATE	X	X	0	X	1
0	QUIESCENT	0	1	0	0	1

24	ILLEGAL STATE	X	X	0	X	1
0	QUIESCENT	0	1	0	0	1

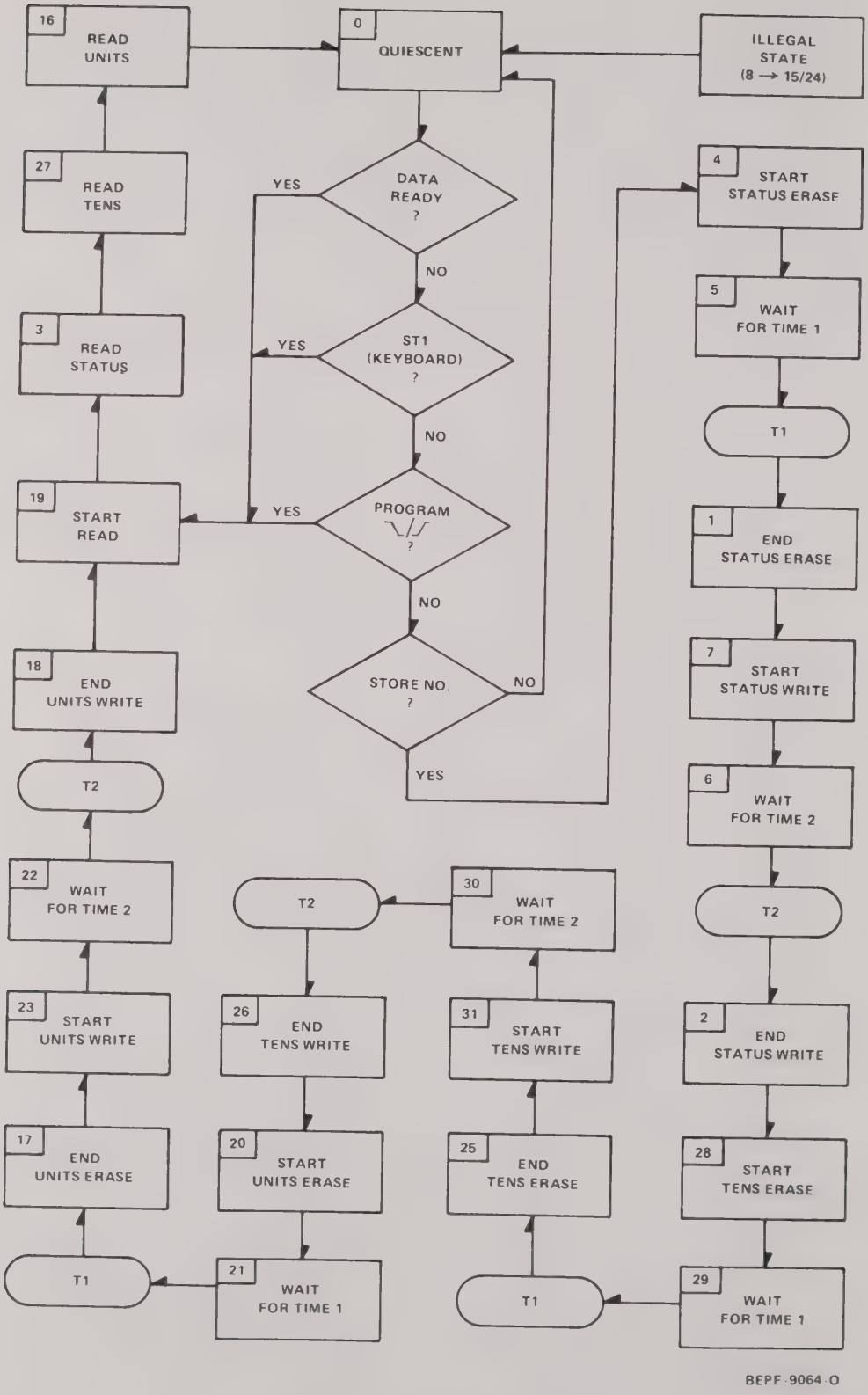


Figure 47. Control State Flow Chart

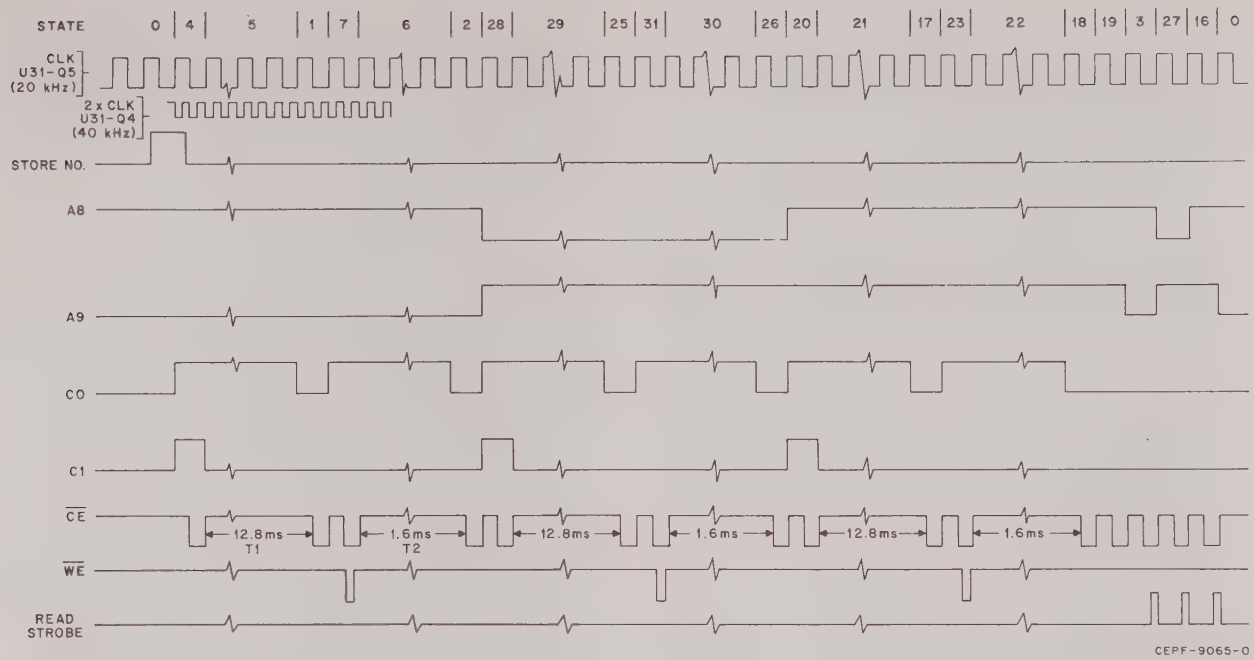


Figure 48. Memory Control Signal Timing

(d) Control State 27 (Read Tens Word)

The conditions for State 27 are similar to State 3, except that A9 = 1 and A8 = 0 due to flip-flops U24A and U35B being in the set state. The combination of A9 = 1, A8 = 0, and C0 = 0 causes the "X0" and "Y0" outputs of analog multiplexers U8 and U9 to be selected. The data bits of the tens word (via the four sense amplifiers) are applied to the "D" inputs of U16, which is clocked by the high output from gate U32C through U20B. When U16 is clocked, the data is applied to the "D" inputs of U15.

Since the "Q3" output of U34 is high in State 27, a high will be applied to the "K" inputs of U35B, U29A, and U29B so that the next clock pulse will cause State 16 to be decoded.

(e) Control State 16 (Read Units Word)

The conditions for State 16 are almost identical to State 27. The units word is addressed because A9 = 1 and A8 = 1. The units data is routed to the "D" inputs of U16 and clocked through to the "Q" outputs in the same manner as the preceding tens word.

The units data is sent to the main terminal board (via J2A, pins 17, 19, 21, and 23) and applied to the "Y" inputs of multiplexer U10. At the same time, the tens data is clocked through U15, sent to the main terminal board (via J2A, pins 16, 18, 20, and 22) and applied to the "X" inputs of multiplexer U10. The "Q6" output of U31 is applied to the "A" and "B" control inputs of U10 to alternately present the tens and units data to the UNI display board for the PAGER NO. display.

The "Q0" output of U28 is high during State 16, producing a high on the "K" input of U24A. With the next clock pulse, all five J-K flip-flops will be reset, and State 0 will be decoded.

(4) Off-Line Operation

NOTE

Whenever the PROGRAM button is depressed or released, and whenever a numeric keyboard number is pressed while PROGRAM is held, a read memory sequence (Control States 19, 3, 27, and 16) is completed and the UNI returns to State 0.

When the PROGRAM button on the UNI front panel is depressed and the terminal is not busy, flip-flop U19A will be set and transistor Q3 will turn on producing the $\overline{\text{LOCKOUT}}$ signal which prevents telephone access to the terminal. Each time a pager code digit is entered via the keyboard, it is presented as BCD information from the display board and applied to the "D" in-

puts of U4 via connector P3, pins 1, 2, 3, and 4. At the same time, a strobe pulse enables gate U13 U13D which clocks the data through to the "D" inputs of U11.

When the second (units) digit is entered, the strobe pulse clocks the tens digit through U11 to the "X" inputs of U6. The units digit is clocked through U4 to the "X" inputs of U7. The data is gated through U4 and U7 to the "Z" outputs because the "A" control inputs are high due to the PROGRAM signal being present.

The "Z" output data from the tens digit multiplexer (U6) is applied to the "X" inputs of the dialed number multiplexer (U5) and to the A4 through A7 address lines of U12. The "Z" output data from the units digit multiplexer (U7) is applied to the "Y" inputs of U5 and to the A0 through A3 address lines of U12.

The tens and units digits are alternately gated through U5 to the DIALED NO. display on the front panel by applying the "Q6" output (10 kHz) of U31 to the "A" and "B" control inputs of U5.

With the dialed number displayed and the same information applied to the A0 through A7 address lines of U12, the UNI is conditioned to process the CHANGE NO. command from the front panel.

(a) Control State 0 (Quiescent)

In the off-line mode, depressing the CHANGE NO. button on the front panel prevents the UNI from leaving State 0 until the STORE NO. button is pressed or the PROGRAM button is released. In State 0, the "Q0" output from U23 (via U18C) enables buffer U3 to pass the keyboard numberic digits to the "D" inputs of U16. When a numeric button is depressed, the keyboard strobe pulse from the display board is used to clock the tens digit through U16 to the "D" inputs of U15.

When the second (units) digit is entered, the strobe pulse clocks the tens digit through U15 to the "X" inputs of U10. The units digit is clocked through U16 to the "Y" inputs of U10. The tens and units digits of the new pager number are alternately gated through U10 to the PAGER NO. display on the front panel by applying the "Q6" output of U31 to the "A" and "B" control inputs of U10.

At the same time that the digits are displayed, the tens digit (word 2) is applied to the "X2" and "Y2" inputs of U8 and U9 and the units digit (word 3) is applied to the "X3" and "Y3" inputs. The status information (word 1) is present at the "X1 " and "Y1" inputs of U8.

When the STORE NO. button is depressed, flip-flop U14B is clocked, enabling gate U25A. The high output from U25A is applied through U22A to the "J" input of flip-flop U35A in preparation for decoding Control State 4 on the next clock pulse.

(b) Control State 4 (Start Status Word Erase)

In State 4, flip-flops U24A and U35B are reset and U35A is set, therefore, A9 = 0, A8 = 1, and C0 = 1. The high Q4 output from U23 is applied to the C1 input of U12, selecting the erase word mode. This same high is routed to the "J" input of U29A so that State 5 will be decoded with the next clock pulse.

(c) Control State 5 (Wait for Time 1)

The "Q5" output from U23 is routed to pin 15 of U12 so that the chip enable pulse ($\overline{CE}$) is inhibited during State 5. This high is also applied to pin 11 of gate U25D, thus preventing changing the state of the J-K flip-flops until the "Q7" output of U37 goes high. When gate U25D is enabled after a 12.8-millisecond delay, a high is applied to the "K" input of U35A and State 1 will be decoded on the next clock pulse.

(d) Control State 1 (End Status Word Erase)

State 1 is used to produce the dummy read operation (C0 = 0 and C1 = 0) required to end the erase cycle and to condition the J-K flip-flops to decode a "7" as the next control state.

(e) Control State 7 (Start Status Word Write)

In State 7, C0 = 1 and C1 = 0 selecting the write mode. The high "Q7" output from U23 enables gate U33C which produces the $\overline{WE}$ pulse. The status word address bits (A9 = 0 and A8 = 1) together with the "C0" bit (C0 = 1) are used to enable the status data at the "X1" and "Y1" inputs of analog switch U8 to pass to the "D0" and "D1" inputs of U12. The $\overline{WE}$ input pulse causes the data on the D0 - D3 input/output lines to be stored in memory.

The high "Q7" output from U23 is also applied through U30D to the "K" input of U29A in preparation for decoding State 6.

(f) Control State 6 (Wait for Time 2)

The "Q6" output of U23 is routed to pin 15 of U12 so that $\overline{CE}$ is inhibited during State 6. This high is also applied to pin 8 of gate

U25C, thus preventing changing the state of the J-K flip-flops until the "Q4" output of U37 goes high. When gate U25C is enabled after a 1.6-millisecond delay, a high is applied to the "K" input of U35A and State 2 will be decoded next.

(g) Control State 2 (End Status Word Write)

State 2 is used to produce the dummy read operation (C0 = 0 and C1 = 0) required to end the write cycle and to condition the J-K flip-flops to decode a "28" as the next control state.

(h) Write Sequence Completion

Words 2 and 3 are stored in memory in the same manner as word 1. The only differences are in next state decoding and memory input line selection through analog switches U8 and U9. The A9 and A8 word address bits determine whether word 2 or word 3 information is present at the D0, D1, D2, and D3 inputs of U12.

The state sequence for the remainder of the write operation is as follows:

STATE	OPERATION
28	Start Tens Word Erase
29	Wait for Time 1
25	End Tens Word Erase
31	Start Tens Word Write
30	Wait for Time 2
26	End Tens Word Write
20	Start Units Word Erase
21	Wait for Time 1
17	End Units Word Erase
23	Start Units Word Write
22	Wait for Time 2
18	End Units Word Write

At the end of the write sequence, State 19 is decoded and a read sequence is completed before the UNI state controller returns to State 0. When the off-line operation is completed and the PROGRAM button is released, the new data is contained in memory at the original dialed number address.

f. NLN5116A UNI Display Board
(Refer to schematic diagram 63E81015C44)

When the PROGRAM button on the front panel is depressed, the PROGRAM command is sent to the UNI primary board, and at the same time, enables gate U1A to light the decimal points in the DIALED NO. display to indicate that the keyboard is enabled, and that any number entered will affect the dialed number. When the pager digits are entered via the keyboard, they are decoded into BCD information and sent to the primary board along with the keyboard strobe pulse.

The CLOCK A signal (J4, pin 11) is the same clock pulse that alternately returns the tens and units data to the display board, therefore, on the positive half-cycle of CLOCK A, transistor Q1 is turned on allowing the tens digit to be displayed by DS1. On the negative half-cycle of the 10 kHz clock, Q3 turns on enabling the DS2 LED to display the units digit.

When the CHANGE NO. button is depressed, the CHANGE LATCH signal is returned from the primary board. This signal enables the INACTIVE and TWO-WAY buttons and moves the decimal points to the PAGER NO. display.

The pager number displayed is the number stored in memory at the location addressed by the dialed number. The current status is displayed by the INACTIVE and TWO-WAY indicators.

An alternate pager number may be entered through the keyboard and as it is entered, the digits will be returned from the primary board to the PAGER NO. display in the same manner as the DIALED NO.

If an active, one-way pager status is to be changed to inactive, the INACTIVE button must be depressed and released. This will clock U9B, resetting U9A, which turns Q7 on and, in turn lights the inactive LED.

When the STORE NO. button is momentarily depressed, the displayed status and pager number will be stored in memory at the location addressed by the dialed number. Releasing the PROGRAM button returns the UNI to on-line operation.

g. NLN5108A Main Circuit Board Without Emergency Page
(Refer to Schematic Diagram 63E81015C57)

(1) Seize Detection

The 500-millisecond SEIZE pulse from the input board enters the main terminal board at P2A-9 and is routed through the one-way/two-way multiplexer (U50) to the "T" input of go-ahead timer U53B. The trailing edge of SEIZE triggers U53B for approximately 550 milliseconds and returns the HOLD DET signal, via U28C and U50, to the input board.

At the same time, analog switch U27A is closed and oscillator U17B is enabled. The 1500 Hz go-ahead tone is sent to the input board, through U8D and U27A, via P2A-3. After the caller dials the pager code digits, the tens and units data is applied at the "X" inputs of multiplexers U26 and U25, respectively and the DATA READY signal is sent to the main terminal board, via P2A-15.

(2) Normal Pager Code Processing

When the DATA READY signal is received, the control signal and pager code processing sequence described in this paragraph will be implemented, provided that the following conditions do not exist:

- Lockout
- Priority Phone In Use
- Inactive Pager Number Dialed
- Station Identification in Process

These conditions will be treated as exceptions to normal pager code processing and their effects on circuit operation will be described in subsequent paragraphs.

The DATA READY signal enters the main terminal board through connector P2A, pin 15 and is relabeled DATA READY' after being delayed by the time constant of R95 and C57. This delay allows the UNI to determine if a pager code is valid or invalid.

The signal VALID•DATA READY', from the output of gate U48B, is applied to the "D" input of the Page Start flip-flop (U56A) and to pin 5 of gate U46B. The 640 kHz CLK pulse is continually setting and resetting the Input On flip-flop (U54A) until the "Q" output goes high with VALID•DATA READY' present. With gate U46B enabled, the signals INPUT ON (U46B output) and ACTIVE (U46A output) are generated.

The ACTIVE signal is fed back through gate U55A to prevent further clocking of the Input On flip-flop. At the same time, transistor Q6 is turned on and energizes relay K1 (ACTIVE), providing the BUSY closure to any terminal sharing the channel. Assuming a lockout condition does not exist for this terminal, ACTIVE will also enable gate U46D and its low output, through gates U37B, U37A, and U48D, will trigger the Monitor Window Timer (U47A) causing its "Q" output to go high for approximately 3.0 seconds. This high output is labeled MON 1.

The MON 1 signal is inverted by U49D to $\overline{\text{MON 1}}$ and applied to the "C" inputs of U45A, U45B, and U56A so that at the end of the monitor cycle, these flip-flops will be clocked. MON 1 is also applied to the "X0" input of one-way/two-way multiplexer U58, and in a one-way system, the Z0 output goes high and is labeled MON.

The MON signal is applied to pin 6 of U57B, turning off transistor Q11 and preventing relay K2 from being energized so that the Transmit contact closure does not exist and the XMIT LED is off. At the same time, transistor Q10 is turned on, lighting the RCV LED and energizing relay K3 to provide the Monitor contact closure.

Also, MON enables gate U35C, generating WAIT 1 through gates U28A and U31B, and HOLD DET 1 through gate U28C. These two signals are sent to the input board via one-way/two-way multiplexer U50. Finally, the MON signal is applied to inverter U34F and through gate U52D to close analog switch U27D, which allows the receive audio to be heard by the caller if the base station channel is busy. Any receive audio will be detected through gates U37B, U37A, and U48D maintaining the monitor window for approximately three seconds after the channel is quiet.

The $\overline{\text{INPUT ON}}$ signal, through gates U57C and U57D, is applied as a low to pin 5 of U57B and when the Monitor Window Timer (U47A) times out, pin 6 of U57B will go low turning on transistor Q11. This lights the XMIT LED and energizes relay K2 which provides the Transmit contact closure. At the same time, transistor Q10 turns off, de-energizing relay K3 and turning off the RCV LED indicator on the front panel.

At the end of the monitor cycle, the "Q" output of U47A goes low and flip-flops U45A, U45B, and U56A are clocked. Since $\overline{\text{ASI ON}}$ is high, the "Q" output from U45A stays high and does not trigger the ASI timer (U53A) and the high "Q" output from U55D resets U47A to prevent any additional monitor cycles. The low "$\overline{Q}$" output from U56A generates the page start ($\overline{\text{PAGE ST}}$) signal, which triggers Tone A Timer U32A. At the same time, analog switch U27D is opened and the WAIT 1 and HOLD DET 1 signals are dropped.

When the "Q" output of U32A goes high, the page start flip-flop (U56A) is reset via gate U31A and the synthesizer enable signals ($\overline{\text{SYNTH EN}}$ and SYNTH EN) are generated. At this time, the tens and units data is applied to group call decoder U24 and tone A/tone B multiplexer U15.

If a group call (tens digit equals units digit) is not decoded, the low output of U23A is inverted by U33D to enable gate U23A is inverted by U33D to enable gate U21B, passing the tens (tone A) data (BCD) through U15 to the A, B, C, and D inputs of U6. When the tone A timer times out, the tone B timer (U32B) is triggered maintaining the synthesizer enable levels, and the units (tone B) data is passed through U15 to U6.

When a group call is decoded, the output of U23A will be high, selecting the units (tone B) data inputs of multiplexer U15. The high from U23A turns off transistor Q3, changing the time constant for U32A so that the combined turn-on time for timers U32A and U32B is approximately eight seconds.

The BCD-to-decimal encoder (U6) provides a decimal equivalent (0-9) of the tone A or tone B data to the address inputs of frequency select ROM's U5, U4, U3, and U2. Tone generation is accomplished primarily by rate generators U14, U13, U12, and U11 with the tone frequency being selected by the BCD outputs of U5, U4, U3, and U2.

Each of the rate generators receives a BCD input from the frequency select ROM's that determines the number of pulses the rate generator will produce from every ten thousand clock pulses applied. The principle involved is that of adding pulses at predetermined intervals such that the number of pulses produced for every ten thousand clock pulses equals the desired output tone frequency times 128 (2.56 MHz clock frequency divided by 2 and then divided by 10,000 = 128f). This method does not produce a train of equally spaced pulses; it yields only the proper number from every ten thousand clock pulses.

The output of the rate generator is routed to the input of both the divide-by-10 circuit (U1A and U10A) and the range select gating circuit (U19A, U19B, U19C, and U19D). If the tone frequency is to be less than 1000 Hz, the range select control output of range select decoder U21D is a logic "one." This disables the bypass function of the range select gating circuit and applies the output of the divide-by-10 circuit to the input of the divide-by-8 circuit. Conversely, if the tone frequency is to be greater than 1000 Hz, the range select control output of the range select decoder is a logic "zero." This enables the bypass function of the range select gating circuit and applies the output of the rate generator directly to the input of the divide-by-8 circuit. This action changes the final output frequency by a factor of ten; therefore, at frequencies less than 1000 Hz, 0.1 Hz accuracy is obtained. For frequencies greater than 1000 Hz, 1.0 Hz accuracy is obtained.

The output of divide-by-8 circuit U10B is routed to digital-to-analog converter U9A, U9B, and U43E when the timing and control circuitry initiates the $\overline{\text{SYNTH EN}}$ signal. The output of the digital-to-analog converter is a stepped waveform resembling a sine wave. Sixteen clock pulses are required to produce one full cycle of the digital-to-analog converter output.

The output of the digital-to-analog converter is coupled through low-pass filter U8A, which shapes the stepped output of the digital-to-analog converter into a near perfect sine wave, to the input of amplifier U8B. The output of U8B (paging tones) is sent to the base station via U34D and U51D.

The SYNTH EN signal, in addition to closing switch U34D to pass the paging tones, enables oscillator U18B which alternately opens and closes switch U27A at a four Hz rate to provide an audible acknowledgment to the caller that the paging tones are being transmitted.

NOTE

The output of gate U20D (SYNTH EN') is delayed so that the voice message cannot be transmitted before the tone decoding circuitry in certain receiving pagers has time to operate.

When the tone B timer (U32B) times out, the SYNTH EN signal goes low, removing the WAIT signal from the input board which enables the voice allotment timer. At the same time, analog switches U34A and U34C are closed to provide the voice audio path to the base station transmitter.

When the allotment timer times out, the $\overline{\text{AT}}$ level goes high (P2A-13) and $\overline{\text{SYNTH CLR}}$ is produced at the output of gate U23B. This signal holds the tone A and tone B timers reset and clears the digital-to-analog registers (U9A and U9B). Also, the high DATA READY level is removed and the board is conditioned to process another pager code.

(3) Lockout Condition

When the terminal is operated off-line (UNI PROGRAM button depressed) or if another terminal sharing the same transmitter is active, the signal $\overline{\text{L.O.}}$ is sent to the input board to prevent telephone (including priority) access to the terminal. At the same time, inverter U43B produces L.O., which turns on transistor Q9, lighting the lockout LED on the front panel.

(4) Priority Phone

When the PRIORITY signal is received, the priority invalid timer (U47B) is enabled and closes analog switch U27C for approximately

four seconds so that the invalid warbling tone is returned to the level phone before the call is dumped by the input board. Priority calls are processed by the main terminal board in the same manner as a normal level call.

NOTE

There is no allotment timer when priority phone is being used.

(5) Inactive Pager

In systems with a UNI, specific pagers may be taken out of service and programmed as inactive. When a pager code with inactive status is dialed, the VALID level (P2A-10) goes low inhibiting gate U48B which prevents processing of the pager digits. The output of U49C (INVALID) combined with DATA READY' closes analog switch U27B and enables the invalid tone oscillator so that a warbling tone is returned to the caller.

(6) Station Identification

An automatic station identification is transmitted initially when power is applied to the terminal and subsequently 25 minutes after a page is transmitted.

When a page is processed, the SYNTH EN level sets ASI control flip-flop U42B and its low $\overline{Q}$ output enables counter U40A to recognize the clock pulses from U41B. Timer U41B is a free running oscillator which produces a clock pulse approximately every 11.6 seconds. After 128 clock pulses (approximately 25 minutes), U56B is clocked and its $\overline{Q}$ output goes high. When the $\overline{Q}$ output of U54A goes high, the signal $\overline{\text{ASI ON}}$ is produced at the output of gate U46C.

NOTE

If a page is being processed, the ACTIVE signal prevents U54A from being clocked ($\overline{Q}$ output low) and $\overline{\text{ASI ON}}$ will be delayed until DATA READY goes low.

$\overline{\text{ASI ON}}$ produces ACTIVE, which is applied to pin 2 of U55A so that U54A cannot be clocked thereby preventing the $\overline{\text{INPUT ON}}$ signal from being produced until the station identification is transmitted. The ACTIVE signal also starts the monitor window timer (U47A) which produces MON 1, to initiate a monitor cycle.

The signal $\overline{\text{ASI ON}}$ is applied to the "D" input of U45A which is clocked at the end of the monitor period to trigger ASI timer U53A for approximately 12 seconds. The ASI signal turns on transistor Q12 which in turn energizes the ASI relay. At the same time, ASI resets flip-flop U42B which prevents ripple counter U40A from recognizing the clock pulses from timer U41B until another SYNTH EN level is produced.

ASI closes analog switches U34B and U34C, allowing the voice ID to be sent to the transmitter via the XMIT AUDIO bus. At the same time, switch U27D is closed so that the voice ID will be heard by anyone attempting to place a page.

h. NLN5109A Main Circuit Board With Emergency Page

(Refer to schematic diagram 63E81015C57)

This board is identical to the NLN5108A board described in the preceding paragraph, except that additional control circuitry is required for detection and priority processing of one or two specific pager codes designated as emergency numbers. The emergency pager codes are programmed as binary numbers by the setting of rocker switches S1 and S2, and a page is initiated by a switch closure across TB4-1 and TB4-3 (emergency page 1) or TB4-2 and TB4-3 (emergency page 2) on the rear of the terminal. The following discussion will assume that emergency page 1 is activated. Emergency page 2 will produce identical results.

When P1-11 goes low, flip-flop U30A is clocked (through optical isolator U62) and produces the signal $\overline{\text{EMG}}$ at the output of U37D. $\overline{\text{EMG}}$ is inverted to EMG by U33B and this high level applied to the "B" control inputs of multiplexers U26 and U25 selects the "Y" data inputs.

The 640 kHz CLK pulse causes the "Q" and "$\overline{Q}$" outputs of U29A to continually switch states until the high "Q" output from U30A is applied to pin 1 of U21A. When gate U21A is enabled (pins 1 and 2 high), pin 3 goes low producing a high on pin 9 of U37C, which prevents U29A from being clocked. The high output from U21C is inverted to produce the signal $\overline{\text{EMG ST}}$ and, at the same time, the high $\overline{Q}$ output from U29A is applied to the "A" control inputs of multiplexers U16 and U17, selecting the "X" data inputs. This allows the tens and units data programmed into switch S1 (EMG PAGE 1) to appear at the "X" and "Y" data inputs of tone A/tone B multiplexer U15.

NOTE

$\overline{\text{EMG}}$ turns on transistor Q2, producing $\overline{\text{L.O.}}$ which dumps any call in process and prevents access to the terminal.

The $\overline{\text{EMG ST}}$ level triggers U41A producing a one-millisecond synthesizer clear ($\overline{\text{SYNTH CLR}}$) signal, which resets the tone A and tone B timers. When the "Q" output of U41A goes low, $\overline{\text{PAGE ST}}$ is generated, triggering tone A timer U32A. The emergency pager code is then synthesized and processed the same as a dialed page.

The SYNTH EN signal applied to gate U36C allows the CLK pulse to maintain U39A in the triggered state, producing EMG XMIT, which turns on transistor Q11, lighting the transmit LED and energizing relay K2. Gate U57A produces $\overline{\text{XMIT}}$ and when SYNTH EN goes low (paging tones transmitted), switch U34D is opened and switches U34A and U34C are closed. This allows the warbling tone to be transmitted for approximately 7.5 seconds following the paging tones.

When U39A times out, EMG XMIT goes low, breaking the audio path to the transmitter. Also, U39B is triggered applying a low to pin 6 of U22B, resetting flip-flop U30A. With U30A reset, the lockout condition is removed and the terminal is conditioned to process subsequent pages.

i. NLN5107A Tape Player and Amplifier Assembly

(Refer to schematic diagram 63B81015C56)

This assembly consists of a cartridge tape player and audio amplifier, which provides previously recorded station identification messages to the transmitter. The tape contains a series of nine-second messages separated by three-second gaps, and runs for a minimum of 13 seconds to ensure that a complete identification is transmitted.

The circuit is controlled automatically by the ASI logic on the main terminal board. When the $\overline{\text{REC RUN}}$ line goes low, relay K1 is energized by the +14 V dc at pin 10 of P6. With K1 energized, 115 V ac is applied to the tape player motor, which starts the playback. The tape head picks up the recorded message which is amplified and applied to the audio output (P6-2). The audio signal is routed to the transmitter via the ASI audio bus on the main terminal board.

The audio amplifier consists of Q1, Q2, and Q3, which operate from the 8 V dc at pin 10 of P6. Transistors Q1 and Q2 form a high gain dc coupled amplifier with standard NAB equalization provided by a feedback network consisting of R4, R8, R9, C4, and C5. The output of Q2 is capacitively coupled to Q3 via C6. The signal is further amplified and coupled by C9 to contacts on relay K1.

j. NLN4300A Two-Way Board

(1) General

A two-way page is processed in the same manner as a one-way page, until after the tones are transmitted and an acknowlegement is returned to the Sending Party. When the Tone B Timer (U32B) on the main terminal board times out, the positive-going edge of the $\overline{\text{SYNTH EN}}$ signal clocks one-way/two-way control flip-flop U42A. If the "D" input of U42A is high, indicating two-way status, the $\overline{\text{ENABLE}}$ signal will be produced at the "$\overline{\text{Q}}$" output, and the high "Q" output will cause the "Y" input lines of multiplexers U50 and U58 to be selected. With the "Y" inputs selected, the two-way board output signals control the operation of the terminal.

The two-way board functions in either the COR or the VOX/VOR mode of operation. In both operational modes, the transmitter remains on after the paging tones are transmitted and the Sending Party should state the message.

In the COR mode of operation, even though the Sending Party is given the first opportunity to speak, transmitter/receiver switching is acutally controlled by the carrier from the Receiving Party's radio. This means that the Receiving Party may initiate and/or maintain their side of the conversation as long as the push-to-talk switch on the radio is depressed, or until the allotment timer times out. The Sending Party may only speak when the Receiving Party is not transmitting. If a carrier is not detected and the Sending Party does not speak for five seconds, the call will be automatically terminated.

In the VOX/VOR mode of operation, the Sending Party must initiate the conversation within five seconds after the paging tones are transmitted. Otherwise, the call will be automatically terminated.

If the Sending Party does speak within the allotted five seconds, the terminal will remain in transmit until two seconds of transmit audio silence is detected or until the allotment timer times out. After this two-second period, the terminal will switch to a search cycle and whichever party speaks first will determine whether the terminal switches to transmit or receive.

The terminal will keep returning to the search cycle after each transmission until the allotment timer times out or until a five-second period of silence is detected. When the allotment timer times out, a warning tone is generated indicating that the call will be terminated in ten seconds.

(2) Control State Decoding

The timing and sequencing of the transmit, receive, and monitor periods is determined by the control state decoder/generator logic in conjunction with the clock pulses from the output of timer U1. Approximately every 9.5 milliseconds, a positive-going pulse is produced at pin 3 of timer U1 and applied to the "C" inputs of J-K flip-flops U15B (2^0), U15A (2^1), U16B (2^2), and U16A (2^3) producing a binary output which is decoded as a state signal by decoders U17 and U18.

State signals are generated in a sequential loop; i.e., the decoded state signal is used to condition the inputs of the J-K flip-flops such that the next clock pulse will cause the state signal for the following operation to be decoded. For example, State 9 (Switch To Monitor) is decoded when the "Q" outputs of U15B (2^0) and U16A (2^3) are high and the "Q" outputs of U15A (2^1) and U16B (2^2) are low, producing a high "Q1" output from decoder U18. This high is fed back to the "J" inputs of U15A and U16B, and with the next clock pulse, State 15 (Monitor Receive Audio) will be decoded (2^0 set = 1, 2^1 set = 2, 2^2 set = 4, and 2^3 set = 8). Figure 3 is a flow chart of two-way operation showing the state generation sequence and the various gating signals associated with each state.

(3) Control State 0 (IDLE)

When the two-way board is not processing a page, the $\overline{\text{ENABLE}}$ signal is high, resetting allotment timer U5 and J-K flip-flops U15A, U15B, U16A, and U16B. The low "Q" outputs from the J-K flip-flops (binary zero) produce a high "Q0" output (State00) from decoder U17. In this idle state, the board is initiallized to process a two-way page in either the COR switching mode (JU1 removed) or the VOX/VOR switching mode (JU1 installed).

(4) COR Switching Mode

When jumper JU1 is removed, the high enable level is removed from pin 5 of gate U12B, preventing J-K flip-flop U16A from being set. With U16A reset, the "Q" output will be low enabling decoder U17, and the "$\overline{Q}$" output will be high inhibiting decoder U18. Therefore, State 4 (Transmit) and State 5 (Receive) are the only two states decoded in the COR switching mode of operation.

(a) Control State 4 (Transmit)

In State 0, the "Q0" output from decoder U17 is applied as a high through gate U14B to the "J" input of flip-flop U16B (2^2). When $\overline{\text{ENABLE}}$ goes low, the next clock pulse from U1 will set U16B, producing a high "Q4" (State 4) output from U17. In State 4, U15B is reset and XMIT is sent to the main terminal board via pin 6.

The high "Q4" output from U17 is applied to pin 2 of U11A. Initially, a carrier should not be detected ($\overline{\text{COR}}$ high) and pin 1 of U11A should be low. This condition produces a low output from pin 3 of U11A and State 4 will exist until one of the following occurs:

- Carrier is detected (STATE 5)
- Five seconds of silence (LOCKOUT)
- Allotment timer times out ($\overline{\text{WARNING}}$)

1. Carrier Detected

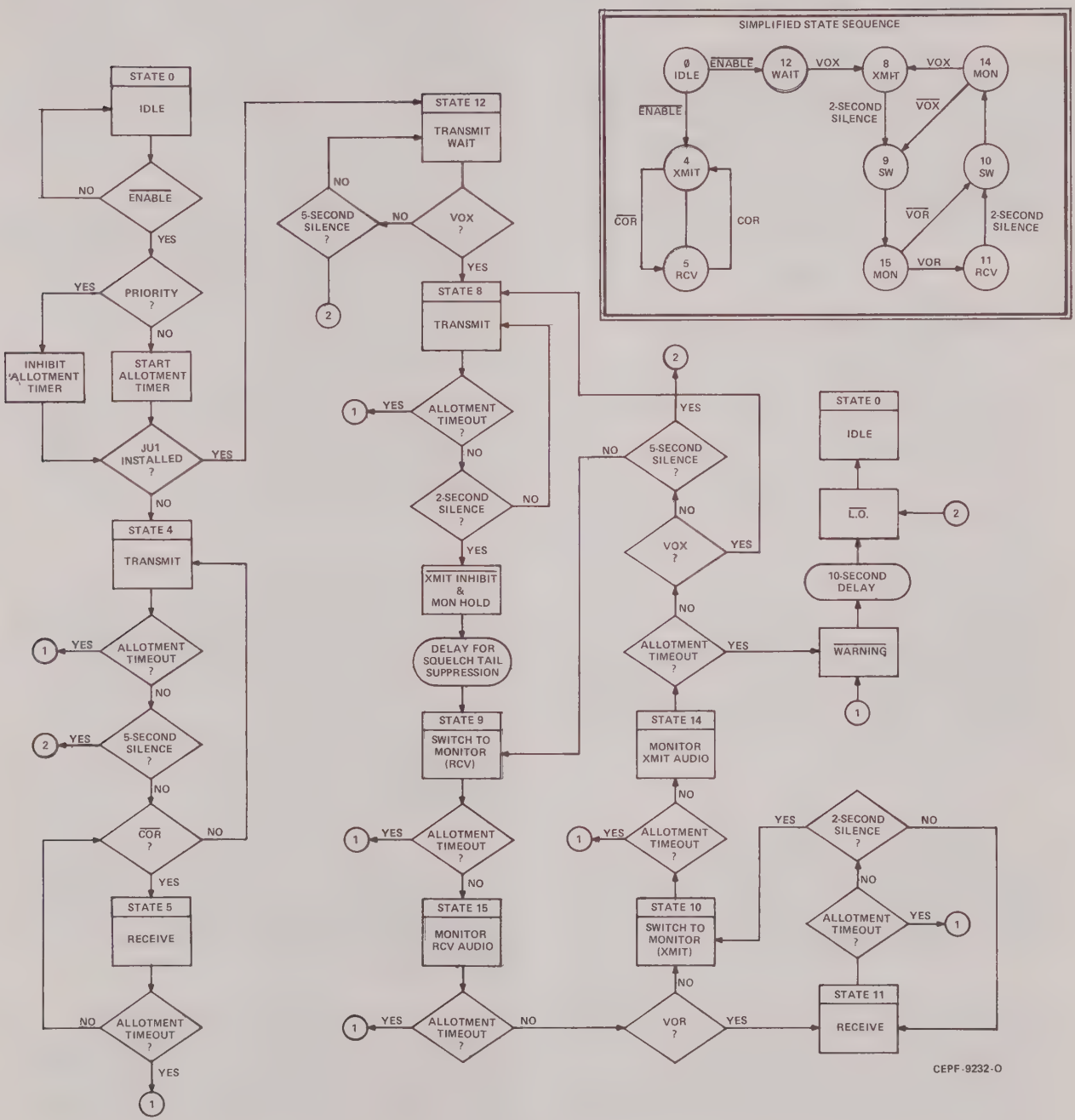
When the Receiving Party keys the radio in response to a call, the carrier detected in the base station receiver provides a relay closure that produces the low $\overline{\text{COR}}$ signal. $\overline{\text{COR}}$ results in a high output from gate U11A that is applied through gate U13C to the "J" input of U15B. The J-K flip-flops are thus conditioned to decode State 5 with the next clock pulse.

2. Five-Second Silence

If no conversation (audio) is detected, the outputs from op amps U3C and U3D will be high, inhibiting gates U10A and U10B, which results in a high output from inverter U7A. This high turns off transistor Q1 and when capacitor C12 charges through R15 (approximately five seconds), pin 1 of op amp U3A will go high, setting flip-flop U8B. The high "Q" output from U8B turns on transistor Q3, producing $\overline{\text{L.O.}}$ and the call is terminated.

3. Allotment Timeout

The 9.5 millisecond clock pulses from U1 are applied to pin 10 of counter U2 and when $\overline{\text{ENABLE}}$ is received, the high reset level is removed from pin 10, allowing the counter to produce a high output from "Q11" every 20 seconds. These 20-second pulses are used to clock counter U5 and, if JU2 is not installed, the "Q3"



Two-Way Functional Flow Chart

output through resistor R24 will go high after 60 seconds. JU2 may be connected to select any of the "Q" outputs from U5 (except "Q3") providing an allotment time ranging from 20 seconds to three minutes.

The high output from U5 is applied to the "D" input of flip-flop U8B and at the same time produces the signal $\overline{\text{WARNING}}$ through inverter U6D. The time-out flip-flop (U8B) is clocked via inverter U6E approximately ten seconds after $\overline{\text{WARNING}}$ is generated. When the "Q" output from U8B goes high, transistor Q3 turns on and $\overline{\text{L.O.}}$ is produced to terminate the call and return the board to an idle state.

NOTE

Allotment timeout will occur and the call will be terminated with $\overline{\text{L.O.}}$ regardless of the current processing state. Only a priority call disables the allotment timer.

(b) Control State 5 (Receive)

When State 5 is decoded, the high "Q5" output from U17 is applied to pin 2 of gate U14A to disable the five- and two-second silence timers and, at the same time is fed back to pin 6 of U11B. Since State 5 is decoded only when $\overline{\text{COR}}$ is low, pin 5 of U11B will be low and the terminal will remain in the receive mode. When the Receiving Party stops transmitting, $\overline{\text{COR}}$ will go high producing a high output from U11B which is applied through gate U13A to the "K" input of U15B. If the allotment timer does not timeout, the next clock pulse will cause State 4 to be decoded.

(5) VOX/VOR Switching Mode

With jumper JU1 installed, gate U12B is enabled and the high "Q0" output from decoder U17 is applied to the "J" inputs of flip-flops U16A and U16B so that with the first clock pulse, State 12 will be decoded.

Note that the "Q" output from U16A is high, disabling decoder U17, and the "$\bar{Q}$" output is low, enabling decoder U18. Since the "K" input to U16A is grounded, this flip-flop will remain set for the entire two-way paging sequence and decoder U18 will generate States 8 through 15 with the following binary inputs.

INPUTS	OUTPUT	STATE
0000	Q0	8
0001	Q1	9
0010	Q2	10
0011	Q3	11
0100	Q4	12
0101	Q5	not used
0110	Q6	14
0111	Q7	15

(a) Control State 12 (Transmit Wait)

When State 12 is decoded, the high "Q4" output from decoder U18 is applied to pin 8 of gate U12C. The controller will remain in State 12 until either five seconds of silence is detected, in which case $\overline{\text{L.O.}}$ will be generated and the call will be terminated, or transmit audio (VOX) is detected.

VOX is used as a clock input to set flip-flop U9B producing a high "Q" output which is applied to pin 9 of gate U12C. This high is applied through gate U14C to the "K" input of flip-flop U16B, and with the next clock pulse, State 8 will be decoded.

(b) Control State 8 (Transmit)

State 8 produces a high "Q0" output from decoder U18 which is applied to pin 13 of gate U11D, and the controller will remain in the transmit mode as long as transmit audio (VOX) is detected via gate U10B, provided allotment time out does not occur. The high output from U10B turns on transistor Q2, which discharges capacitor C13 maintaining a low output from op amp U3B.

When the Sending Party stops talking, pin 14 of op amp U3D goes high producing a low output from gate U10B, which turns off transistor Q2. With Q2 off, capacitor C13 will charge in approximately two seconds producing a high output from op amp U3B.

This high enables gate U11D, causing the signals $\overline{\text{XMIT INHIBIT}}$ and MON HOLD to be sent to the main terminal board. At the same time, the high output from U11D through inverter U6F enables counter U4.

The 9.5 millisecond clock pulses from U1 are applied to pin 10 of counter U2 to produce a series of 38 millisecond pulses at the "Q2" output. These pulses produce a high output from counter U4 depending on the placement of JU3, or if JU3 is not installed, "Q5" will go high approximately 600 milliseconds after U4 is enabled. This delay prevents switching to State 9 until the squelch tail generated by the carrier is dropped. Otherwise, the squelch tail could be detected as received audio.

The high output from U4 is applied through gate U13C to the "J" input of U15B. With the next clock pulse, State 9 will be decoded.

(c) Control State 9 (Switch To Monitor)

When State 9 is decoded, the high "Q1" output from decoder U18 resets U9A and is fed back to the "J" inputs of flip-flops U16B and U15A so that, if allotment timeout does not occur, the next clock pulse will cause State 15 to be decoded.

(d) Control State 15 (Monitor Receive Audio)

In State 15, the high "Q7" output from decoder U18 is applied to the "K" input of U16B through gate U14C and to pin 2 of gate U12A. The next clock pulse will cause either State 10 or State 11 to be decoded, depending on the set or reset condition of flip-flop U9A.

If receive audio (VOR) is detected, U9A will be clocked to the set condition and State 11 will be decoded. If there is no voice response from the Receiving Party, the "$\overline{Q}$" output of U9A will be high enabling gate U12A to reset U15B causing State 10 to be decoded.

(e) Control State 11 (Receive)

When State 11 is decoded, the high "Q3" output from U18 is applied to pin 8 of gate U11C, and the controller will remain in the receive mode as long as receive audio (VOR) is detected, provided that the allotment timer does not time out.

When the Receiving Party stops talking, pin 8 of op amp U3C goes high, producing a low output from gate U10A, which turns off transistor Q2. With Q2 off, capacitor C13 will charge in approximately two seconds producing a high output from op amp U3B. This high enables gate U11C and its high output is applied through gate U13A to the "K" input of U15B. With the next clock pulse State 10 is decoded.

(f) Control State 10 (Switch To Monitor)

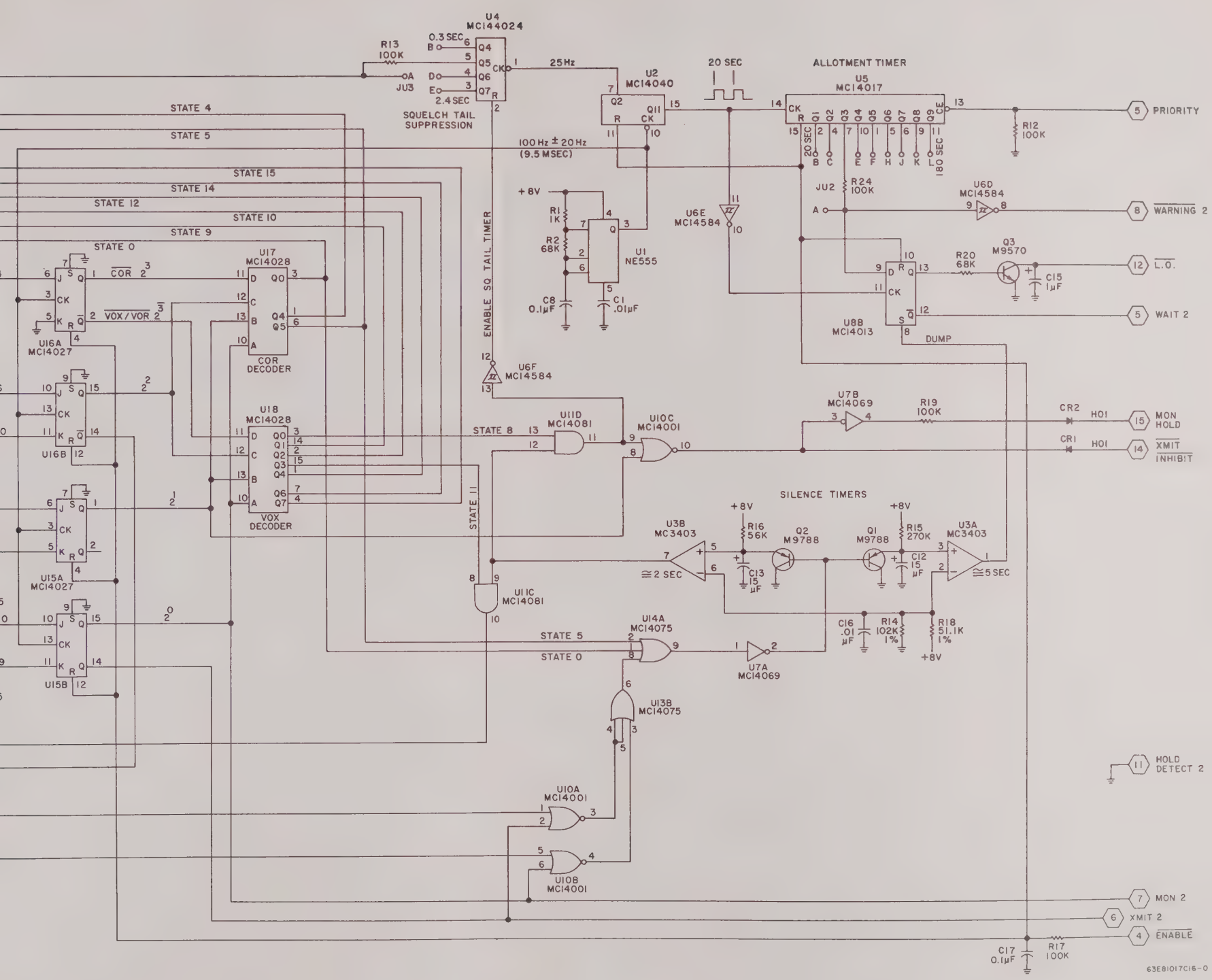
In State 10, the "Q2" output of decoder U18 goes high and is fed back to the "J" input of U16B through gate U14B. If the allotment timer does not time out, the next clock pulse will cause State 14 to be decoded.

(g) Control State 14 (Monitor Transmit Audio)

In State 14, the "Q6" output from decoder U18 is applied to the "K" inputs of flip-flops U16B and U15A and to pin 12 of gate U12D. The next clock pulse will cause either State 8 or State 9 to be decoded, depending on the set or reset condition of flip-flop U9B.

If transmit audio (VOX) is detected, U9B will be clocked to the set condition and State 8 will be decoded. If there is no voice audio from the Sending Party, the "$\overline{Q}$" output of U9B will be high, enabling gate U12D to set U15B, causing State 9 to be decoded.

NOTES



UNLESS OTHERWISE STATED:
VALUES ARE IN OHMS, k = 1000;
OR VALUES ARE IN MICROFARADS (uF);
R VALUES ARE IN HENRYS (H).

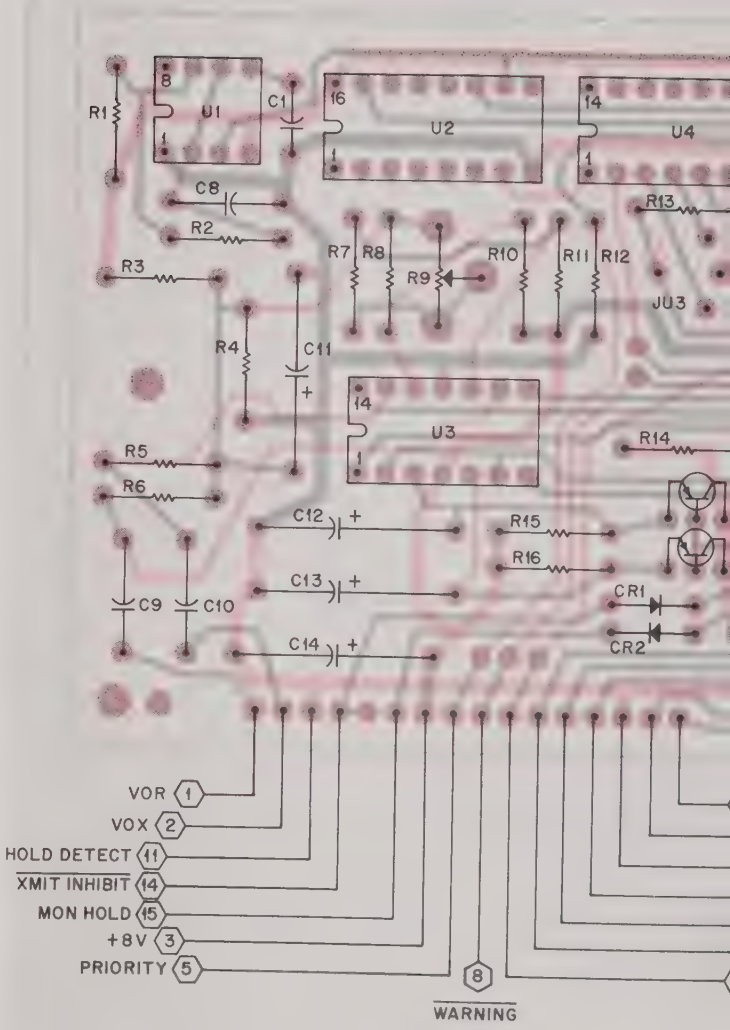
EPF-7506-O

NLN4300A TWO-WAY BOARD
SCHEMATIC DIAGRAM

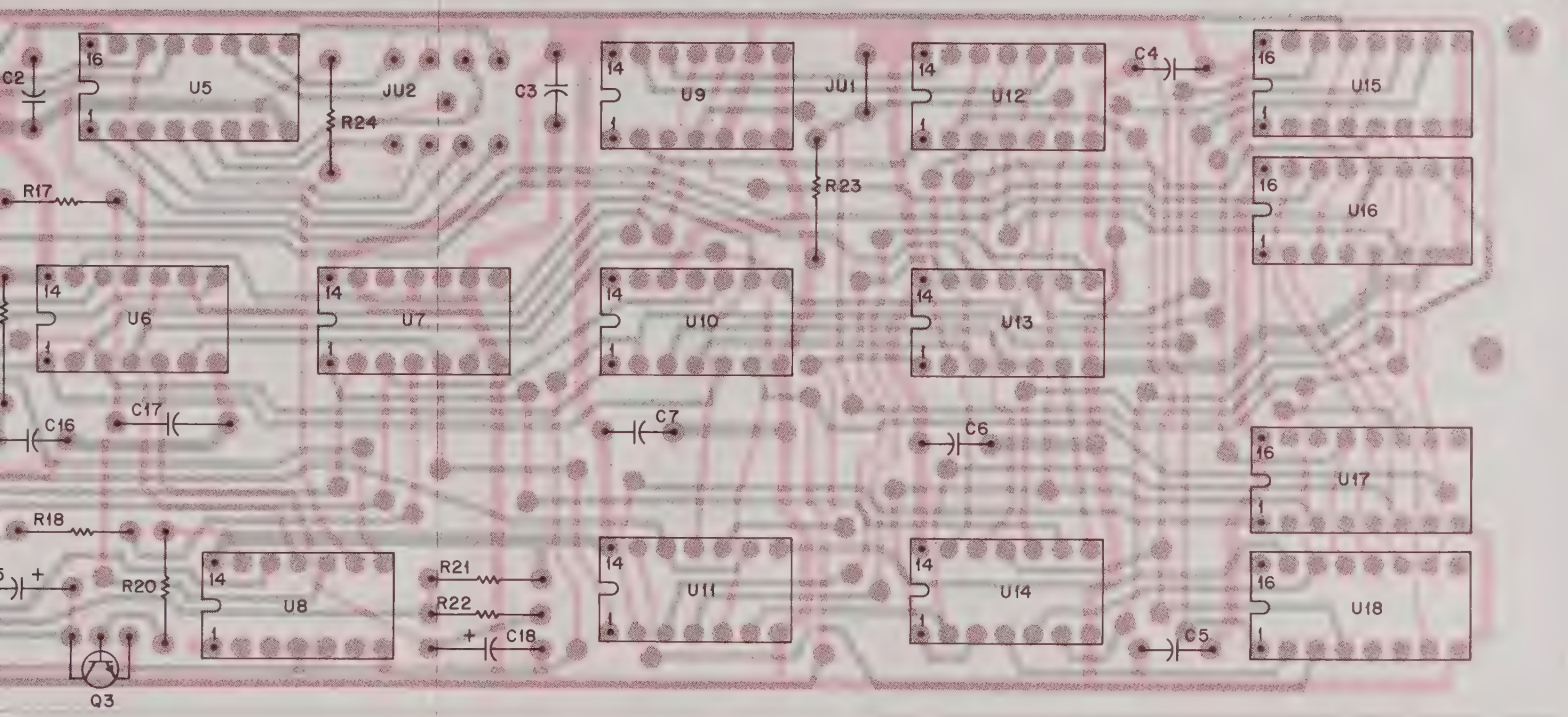
NLN4300A Two-Way Board Kit PLF-1511-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		CAPACITOR, Fixed: uF ±10%; 250 V unless stated
C1 thru 7	2182428B04	.01 -30+70%; 100 V
C8, 9, 10	0882096J18	0.1
C11 thru 14	2383214C16	15 ±5%; 20 V
C15	2383397D10	1 ±20%; 25 V
C16	2182428B04	.01 -30+70%; 100 V
C17	0882096J18	0.1
C18	2383397D10	1 ±20%; 25 V
		DIODE: See Note
CR1, 2	4883654H01	Silicon
		TRANSISTOR: See Note
Q1, 2	4800869788	PNP; type M9788
Q3	4800869570	NPN; type M9570
		RESISTOR, Fixed: Ω ±5%; 1/4 W unless stated
R1	0600124A49	1 k
R2	0600124A93	68 k
R3, 4	0600124A63	3.9 k
R5, 6	0600124A73	10 k
R7	0600124A35	270
R8	0600124A73	10 k
R9	1883083G10	Pot., 10 k
R10	0600124A97	100 k
R11	0600124A89	47 k
R12, 13	0600124A97	100 k
R14	0684444A26	102 k ±1%
R15	0600124B08	270 k
R16	0600124A91	56 k
R17	0600124A97	100 k
R18	0683175C60	51.1 k ±1%
R19	0600124A97	100 k
R20	0600124A93	68 k
R21	0600124A73	10 k
R22	0600124A89	47 k
R23, 24	0600124A97	100 k
		INTEGRATED CIRCUIT: See Note
U1	5184320A35	Timer, type 555
U2	5182822F46	CMOS, type MC14040
U3	5184621K21	Quad Operational Amplifier, type MC3403
U4	5184887K34	CMOS, type MC14024
U5	5184887K33	CMOS, type MC14017
U6	5184887K52	CMOS, type MC14584
U7	5184887K11	CMOS, type MC14069
U8, 9	5184887K13	CMOS, type MC14013
U10	5184887K09	CMOS, type MC14001
U11, 12	5182822F44	CMOS, type MC14081
U13, 14	5184887K29	CMOS, type MC14075
U15, 16	5184887K21	CMOS, type MC14027
U17, 18	5184887K20	CMOS, type MC14028
		NONREFERENCED ITEMS
	0482418B16	WASHER, Insulating
	0400001719	WASHER, Flat
	0400007669	LOCKWASHER, #6
	3782603D01	SLEEVE, #1
	3782603D02	SLEEVE, #2
	3782603D03	SLEEVE, #3
	3782603D04	SLEEVE, #4
	3782603D05	SLEEVE, #5
	3782603D06	SLEEVE, #6
	3782603D07	SLEEVE, #7
	3782603D08	SLEEVE, #8
	3782603D09	SLEEVE, #9
	3782603D10	SLEEVE, #10
	3782603D11	SLEEVE, #11
	3782603D12	SLEEVE, #12
	3782603D13	SLEEVE, #13
	3782603D14	SLEEVE, #14
	3782603D15	SLEEVE, #15
	4210217A02	TIE WRAP
	4305507G01	STANDOFF
	8405524G01	CIRCUIT BOARD

NOTE: For optimum performance, order replacement diodes, transistors, and integrated circuits by Motorola part number only.



VIEWED FROM COMPONENT SIDE



MON
XMIT
10 GND
2 L.O.
13 COR
WAIT
ENABLE

SS - EEPF - 9198 - 0
CS - EEPF - 9199 - 0
OL - EEPF - 9200 - 0

INTEGRATED CIRCUIT VOLTAGE
& GROUND PIN DESIGNATIONS

REF. DES.	TYPE NUMBER	+V	GND
U1	NE555	8	1
U2	MC14040	16	8
U3	MC3403	4	11
U4	MC14024	14	7
U5	MC14017	16	8
U6	MC14584	14	7
U7	MC14069	14	7
U8, 9	MC14013	14	7
U10	MC14001	14	7
U11, 12	MC14081	14	7
U13, 14	MC14075	14	7
U15, 16	MC14027	16	8
U17, 18	MC14028	16	8

AEPF-9201-O

		VOX/VOR	COR
JU1		IN	OUT

JU2		ALLOTMENT TIMER
A	TO	B = 20 SEC.
A	TO	C = 40 SEC.
A	TO	NONE = 60 SEC.
A	TO	E = 80 SEC.
A	TO	F = 100 SEC.
A	TO	H = 120 SEC.
A	TO	J = 140 SEC.
A	TO	K = 160 SEC.
A	TO	L = 180 SEC.

JU3		SQUELCH TAIL SUPPRESSION
A	TO	B = 300 mSEC
A	TO	NONE = 600 mSEC.
A	TO	C = 1.200 mSEC.
A	TO	E = 2.400 mSEC.

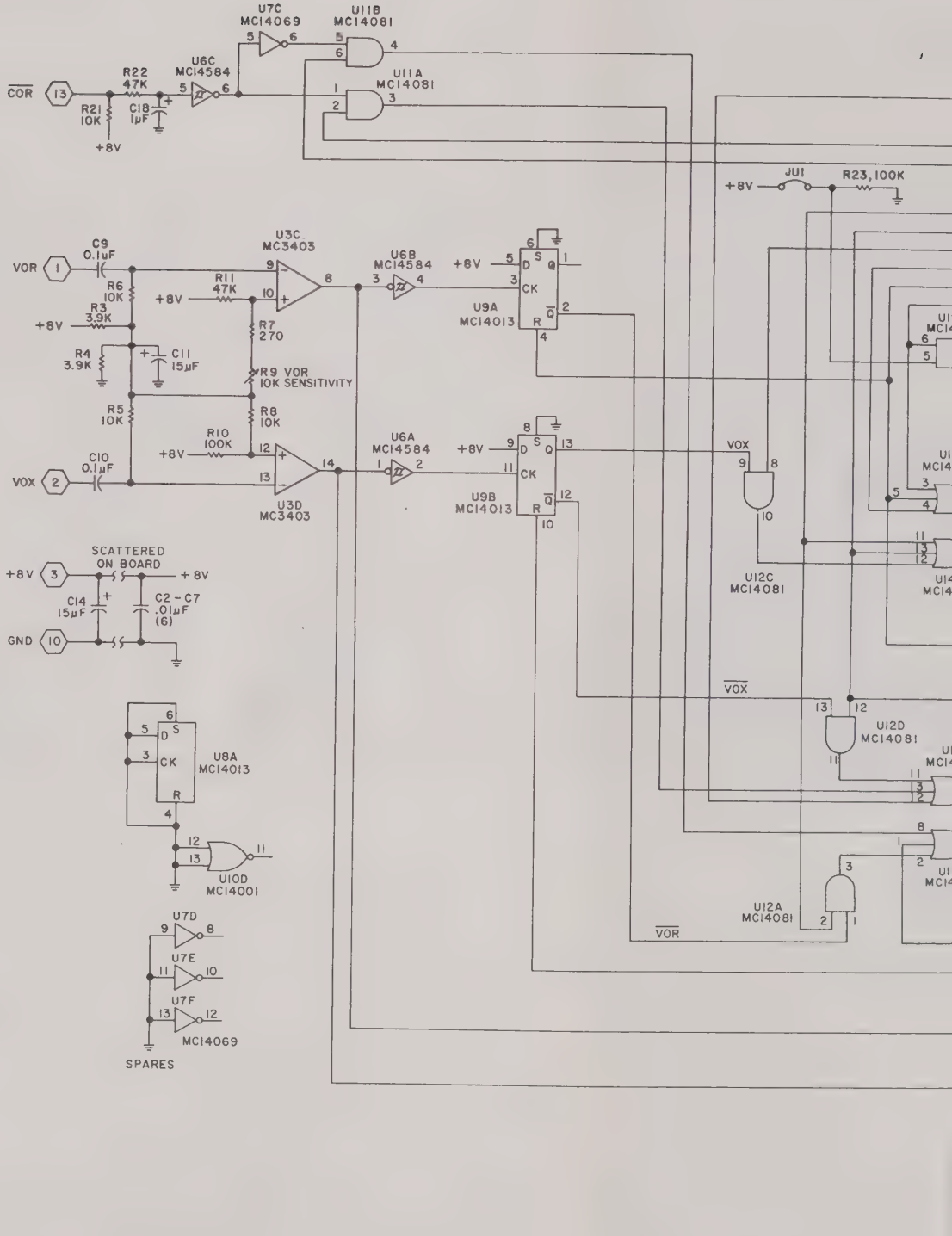
VOR - VOICE OPERATED RECEIVE
VOX - VOICE OPERATED TRANSMIT
COR - CARRIER OPERATED RELAY

EPF 9276 O

CONNECTOR INFORMATION

NUMBER	CONNECTS TO / FROM
J / P 1	CHASSIS / MAIN TERMINAL BOARD
J2 / P2 P2A	INPUT BOARD / UNI MAIN MAIN TERMINAL BOARD
J / P 3, 4	MAIN UNI BOARD / UNI DISPLAY BOARD
J / P 5	KEYBOARD / UNI DISPLAY BOARD
J / P 6	CHASSIS / ASI
J P 7	CHASSIS / INPUT BOARD
P8 J8 J8A	INPUT BOARD / CHASSIS CABLE TO J9
J9 P9	CABLE / L.L. INTERFACE BOARD

EPF-9294-O



NOTES
RESIST
CAPAC
INDUC

MAINTENANCE

1. INTRODUCTION

This section describes recommended repair procedures, special precautions regarding maintenance, recommended test equipment, and system troubleshooting techniques. Each of these topics provides information vital to the successful operation and maintenance of the "MODAX" 100 Paging Terminal described in this manual.

2. PREVENTIVE MAINTENANCE

a. Visual Inspection

Check that external surfaces of the equipment are clean, that connecting cables and wires are not damaged, and that connections are firm. A detailed inspection of the interior electronic circuits is not needed or desired.

b. Cleaning

Periodically clean smudges and grime from the the exterior of the housing. Use a soft, non-abrasive cloth moistened in a mild soap and water solution. Rinse the surface using a second cloth moistened in clean water.

3. DISASSEMBLY

The terminal top cover may be raised for access to the circuit boards by removing the two screws located toward the front panel, one on each side of the housing. The following paragraphs describe the removal of the individual circuit boards. Figure 49 shows the chassis and board intercabling for reference during disassembly and reassembly of the terminal.

a. Main Terminal Board Removal

Unplug the two 23-pin connectors (J1 and J2/J2A) and remove the six screws and associated washers that secure the board to the terminal top cover. The screws are located three on each side of the board.

b. Input Board Removal

Unplug the 23-pin connector (J2) and remove the main terminal board so that the J2 wiring harness does not have to be worked out from under the board. Removing the main terminal board also simplifies reinstallation of the cable.

Unplug the two 15-pin connectors (J7 and J8/J8A) and remove the four corner screws and associated washers that secure the input board to the standoffs on the bottom of the housing.

c. Main UNI Board Removal

Unplug the two 23-pin connectors (J2 and J2A) and the two 15-pin connectors (J3 and J4). Remove the six screws and associated washers that secure the board to the terminal top cover. The screws are located three on each side of the board.

d. UNI Display Board

Remove the input, main terminal, and main UNI boards to provide access to the J3-J4 wiring harness. Remove the tie wraps that tie the harness to other chassis wiring (under the input board) and unfasten the plastic cable clamps that secure the cable at TB4 and TB6 on the rear panel.

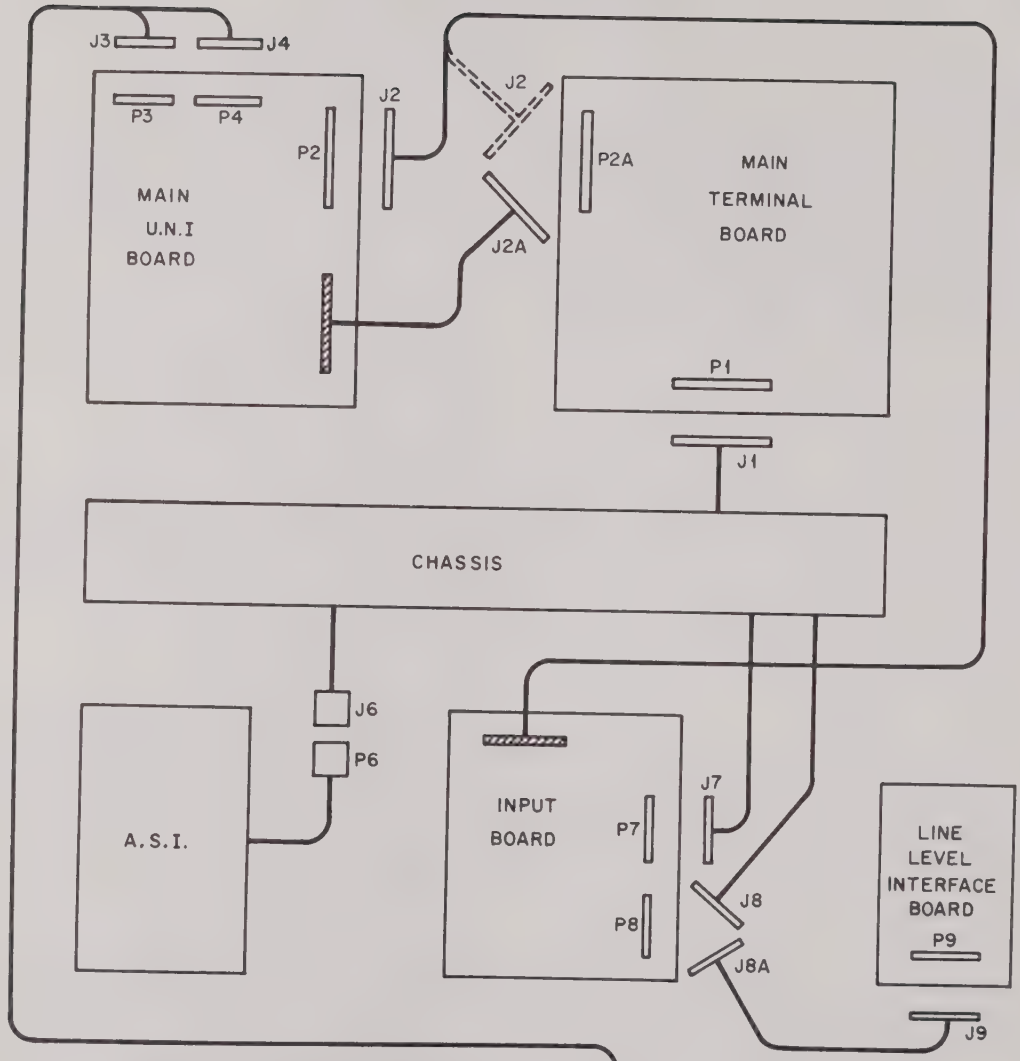
Remove the four screws and associated washers that secure the display board to the standoffs on the front panel. Move the board away from the front panel and unplug connector J5.

NOTE

The line level interface board should be removed if your terminal is so equipped to provide access to the screw in the lower corner of the terminal.

e. UNI Keyboard Removal

Remove the four screws and associated washers that secure the display board and move the display board aside. Unplug connector J5



ALTERNATE CONNECTIONS		
CONNECTOR	MATES WITH	CONDITION
J2	P2A	NO U.N.I.
	P2	U.N.I.
P2A	J2	NO U.N.I.
	J2A	U.N.I.
P8	J8	SELECTOR LEVEL
	J8A	LINE LEVEL

Figure 49. Terminal Intercabling Detail

and remove the four nuts that secure the keyboard to the front panel. To completely remove the keyboard, unsolder the wires from connector J5 to the PROGRAM, INACTIVE, and TWO-WAY switches and indicators.

f. Line Level Interface Board Removal

Unplug connector J9 and remove the RED and GRN telephone cable wires that are attached to two screw terminals on the board. The board should be removed with its two mounting brackets attached by removing the hardware that fastens the brackets to the bottom of the housing.

g. ASI Tape Removal

Remove the two screws on the rear of the terminal housing that hold the tape access cover in place and remove the cover. The tape may then be removed and/or inserted the same as any standard eight-track cartridge.

h. ASI Tape Player Removal

The entire tape player assembly is removed as a unit. Separate connectors J6 and P6, and remove the four screws that secure the assembly to the bottom of the terminal housing.

i. Audio Amplifier Board Removal

The audio amplifier board is located on the front panel directly behind the speaker grille. Unplug the seven wires and remove the two nuts and washers that secure the board to the front panel studs.

4. TROUBLESHOOTING

Servicing of the paging terminal requires the localizing of the malfunctioning circuit before the defective component can be isolated and replaced. Since localizing and isolating a defective component constitutes the most time-consuming part of troubleshooting, a thorough understanding of the circuits involved will aid the technician in performing efficient servicing. The technician must know how one function affects another; he must be familiar with the overall operation of the encoder and the procedures necessary to place it back in operation in the shortest possible time.

The paging terminal functional diagrams, schematic diagrams, and troubleshooting charts provide valuable information for troubleshooting purposes. The functional diagram provides signal flow information in a simplified format while the schematic diagram provides the detailed circuitry and the biasing voltages required for isolating malfunctioning components. The troubleshooting charts further isolate malfunctioning components. Generally, it may be assumed that if the paging terminal is totally inoperative, the power inputs or power supply is defective. However, if the terminal operates in the transmit mode but not in the receive mode (or vice versa), it may be assumed that the power supplies are serviceable and that one or more functional circuits are defective or marginal. By using the diagrams, troubleshooting charts, and deductive processes, the suspected circuit may be readily found.

Table 25. System Troubleshooting Chart - Priority Phone Input

TROUBLE INDICATION	POSSIBLE PROBLEM AREA
Busy LED does not light with phone lifted off-hook.	PRIORITY signal not generated on input board.
No Go-Ahead tone received.	a. SEIZE pulse not generated on input board or present on main board. b. Edge of SEIZE pulse not detected on main board. c. Transmit audio path open on main or input board.
Acknowledge (beeping) tone not heard when pager code is dialed.	a. DATA READY signal not generated on input board or present on main board. b. SYNTH ENABLE signal missing on main board. c. Transmit audio path open on main or input board.
Paging tones not transmitted or heard through front panel speaker.	a. Tone or dial decoding circuit not functioning on input board. b. No paging tone output from synthesizer circuitry on main board. c. Transmit audio path open or audio amplifier board defective.
Voice message not transmitted or heard through front panel speaker.	Open audio path through input board analog gates to main board agc and out to audio amplifier board and rear panel.
Priority phone does not dump level phone.	Reset one-shot on input board not triggered by PRIORITY signal.

Table 26. System Troubleshooting Chart - PABX Phone Input

TROUBLE INDICATION	POSSIBLE PROBLEM AREA
Busy signal returned when access code is dialed.	a. OH1 low on line level input board. b. COS relay open on selector level input board.
Ringing but system does not answer.	Line Level Input: a. RU1 pulse input missing. b. OH1 high. c. Interface board not operating. Selector Level Input: a. S1 input high. b. CS/ER1 relay defective. c. Missing SEIZE pulse.
No Go-Ahead tone returned.	a. Negative edge of SEIZE pulse not detected on main board. b. 1.5 kHz oscillator inoperable. c. Audio path open on main or input board.
Acknowledge (beeping) tone not heard when pager code is dialed.	a. DATA READY signal not generated on input board or present on main board. b. SYNTH ENABLE signal missing. c. 4 Hz or 1.5 kHz oscillator defective. d. Audio path open on main or input board.
Paging Tones not transmitted or heard through front panel speaker.	a. Decoder circuitry on input board not functioning properly. b. No paging tone output from synthesizer circuitry on main board. c. Transmit audio path open or audio amplifier board defective.
Voice message not transmitted or heard through front panel speaker.	a. No AK1 relay closure (DCW dial selector level). b. Open audio path.
Premature time-out during voice period.	a. Missing 640 kHz CLK signal. b. Missing WAIT signal during paging tone transmission. c. Defective allotment timer circuit component.
Time-out does not occur.	a. WAIT signal present. b. Generation of AT1 closure (DCW only) at end of allotment period.
Pressing PROGRAM button on UNI, emergency page, or L.O. grounded on rear panel does not prevent incoming calls.	$\overline{\text{LO}}$ missing on input or main terminal board.
System does not leave monitor period.	a. Noise on RCV AUDIO. b. RCV AUDIO potentiometer adjusted for too high sensitivity.
Audio heard through front panel speaker but not transmitted.	No PTT closure to base transmitter.

Table 27. UNI Troubleshooting Chart

TROUBLE INDICATION	POSSIBLE PROBLEM AREA
DIALED NO. decimal points fail to light when PROGRAM button is pressed and held.	a. Check J3, pin 13. If this signal is low immediately after PROGRAM is pressed, the problem is on the display board. b. Otherwise, the problem is on the UNI main board.
Decimal points fail to change when CHANGE is pushed while PROGRAM is held.	a. Check J3, pin 13. If this signal is high, the problem is on the display board. b. Check J3, pin 14. This signal should go high when CHANGE is pushed. If it does, the problem is on the UNI main board. c. Check the pushbutton switch and associated wiring.
One column of the LED displays functions, but not the other.	a. Check for a 10 kHz square wave at J4, pin 11. If this signal is not present, check J3, pin 6 for a 640 kHz square wave. If present, the fault is on the UNI main board. If not, the problem is on the main terminal board. b. If the 10 kHz clock is present at J4, pin 11, check that correct BCD data is being presented to the display board from the main terminal board. If the data is correct, the fault is on the display board. Otherwise, check the main terminal board.
LED displays do not light.	a. Check +8V on display board. b. Check that valid BCD data is being presented from the UNI main board.
LOCKOUT does not light when PROGRAM is pushed and held.	a. If J3, pin 7 does not go low when PROGRAM is pushed, check the display board. b. Otherwise, check the UNI main board and the LED.
Data does not store when STORE is pushed.	a. If the LED displays worked properly while the data was being set up, the problem will be found on the UNI main board. b. Check the power supply voltages on U12.
Data does not enter properly from the keyboard.	a. Check that properly encoded BCD data and data strobe is generated on the display board. b. The same BCD data should be passed back from the UNI main board to the displays on the display board.
UNI is suspected of causing incorrect paging operations.	a. Disconnect J2A from the main terminal board and J2 from the UNI board. Reconnect J2 to P2A on the main terminal board. This will remove the UNI from the rest of the paging system. b. If the UNI board was at fault, paging will now occur normally although no number interchanges may take place. The LED displays will be off in this configuration.

5. RECOMMENDED TEST EQUIPMENT

The following items, or their equivalent, must be available for proper installation and maintenance of the paging terminal:

EQUIPMENT	PURPOSE
Service Monitor - Motorola Model R1200	Check deviation of paging tones
Oscilloscope, Dual - Trace - Tektronix T922	Check audio distortion and monostable timing
VOM - Motorola Model R1001A	DC Measurements
Frequency Counter - Motorola Model S1357	Check tone frequencies
AC Voltmeter - Motorola Model S-1053C	Set input and output levels

The following items, or their equivalent, are optional, but will aid you to minimize down time when troubleshooting the paging terminal:

EQUIPMENT	PURPOSE
Logic Monitor Clip - Hewlett Packard Model 548A	Simultaneously monitor and display all pins of a DIP IC package
Logic Pulser - Hewlett Packard Model 546A	Inject pulses into logic nodes without cutting lands or removing IC's
Current Tracer - Hewlett Packard Model 547A	Locate stuck voltage nodes
Logic DIP Clip - Motorola ST-1190 or or equivalent	Extend IC pins from the board to connect scope or test equipment and avoid shorting IC pins to adjacent parts

6. MOS HANDLING PRECAUTIONS

MOS (Metal Oxide Semiconductor) devices are used in the paging terminal. While the attributes of MOS type devices are many, their characteristics make them susceptible to damage by electrostatic or high voltage charges. Therefore, when the service technician encounters MOS circuits, special precautions to prevent device damage must be taken during repair procedures outlined in the following sections. The following handling precautions are recommended for MOS circuits and are especially true in dry-humidity conditions.

a. Store and transport all MOS devices in conductive material so that all exposed leads are shorted together. Do not insert MOS devices into conventional plastic "snow" or plastic trays of the type used for storage and transportation of other semiconductor devices.

b. Ground the working surface of the service bench to protect the MOS device.

c. Wear a conductive wrist strap in series with a 100 k resistor to ground.

d. Do not wear nylon clothing while handling MOS devices.

e. Neither insert nor remove MOS devices with power applied. Check all power supplies to be used for testing MOS devices and be certain there are no voltage transients present.

f. When straightening MOS leads, provide ground straps for apparatus used.

g. When soldering, use a grounded soldering iron.

h. If at all possible, handle all MOS devices by the packages and not by the leads. Prior to touching the unit, touch an electrical ground to remove any static charge that you may have accumulated. The package and substrate may be electrically common. If so, the reaction of a discharge to the case would cause the same damage as touching the leads.

7. REPAIR PROCEDURES

a. Parts and Substitution

When damaged parts must be replaced, identical parts should be used. If the identical replacement component is not locally available, check the parts list of the respective printed circuit board for the proper Motorola part number and order the components from the nearest Motorola Replacement Parts Depot as listed in the "Replacement Parts Ordering" section of this instruction manual. If for any reason substitutions must be made immediately, it is recommended that the substitutions be replaced as soon as the proper replacement part is available. The substituted part must have identical electrical properties and must be of equal or higher voltage and current ratings.

b. Component Removal

Most components are located on circuit boards. Special care should be taken during troubleshooting to be as certain as possible that the suspected component is actually the one at fault. The special care will eliminate unnecessary unsoldering and removal of parts which may damage or weaken other components or the circuit board itself.

CAUTION

MOS integrated circuits are used extensively throughout the system; use special care when handling these devices. See "MOS Handling Precautions" paragraph in this section.

Use of a 40-watt pencil type soldering iron is recommended. The Motorola ST-639 Printed Circuit Repair Kit contains a recommended 40-watt iron as well as soldering aids (probers), magnifying glass, solder, solvent, and brush. A solder remover of the squeeze-bulb type such as the ST-726 is also recommended. Use an iron with a tapered point to permit its exact application to the desired connection in compact equipment. Always keep the soldering iron tip well tinned and clean.

c. Soldering

Before soldering any connections, carefully scrape all parts to be soldered until all traces of rust, corrosion, paint or varnish are removed. Dust the scraped parts with a small clean brush. Tin all surfaces to be soldered. Wrap the wire around the lug to be soldered to obtain sufficient mechanical support (if applicable). Solder the connection, using a minimum amount of solder with sufficient heat to make the solder flow evenly around the tinned surface.

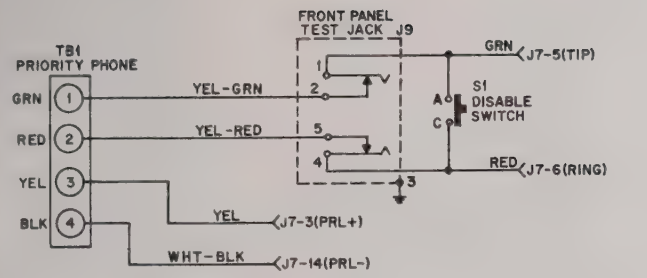
d. Printed Circuit Repair Techniques

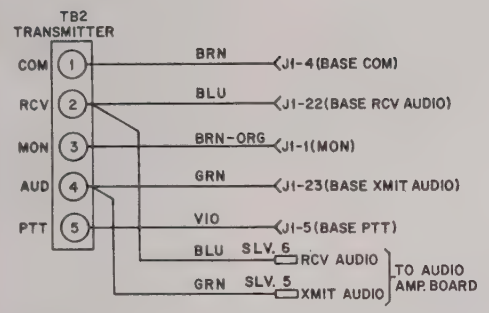
Using a soldering iron with low heat output, in many cases, has actually caused damage that the serviceman was trying to prevent while repairing printed circuits. It is absolutely necessary to raise the temperature of the connection until the solder flows freely around the board eyelet. This usually takes a considerable amount of time with a very low heat iron. During this time heat is conducted away from the connection by the printed wiring causing it, in some instances, to break away from the board. If a component is to be removed, its soldered connections must be raised to a temperature that permits free flow of solder. Otherwise the component leads may not be freed from the printed wiring and the wiring will be pulled loose from the board as the component is removed. The soldering iron supplied with the Motorola Printed Circuit Repair Kit is recommended for most work on printed circuit boards. This high-heat iron need be applied only a very short time to heat a connection to the point where solder flows freely. It is obvious that an iron this hot should not be held on a connection longer than necessary. Extended periods of high heat will cause the foil to peel loose from the board.

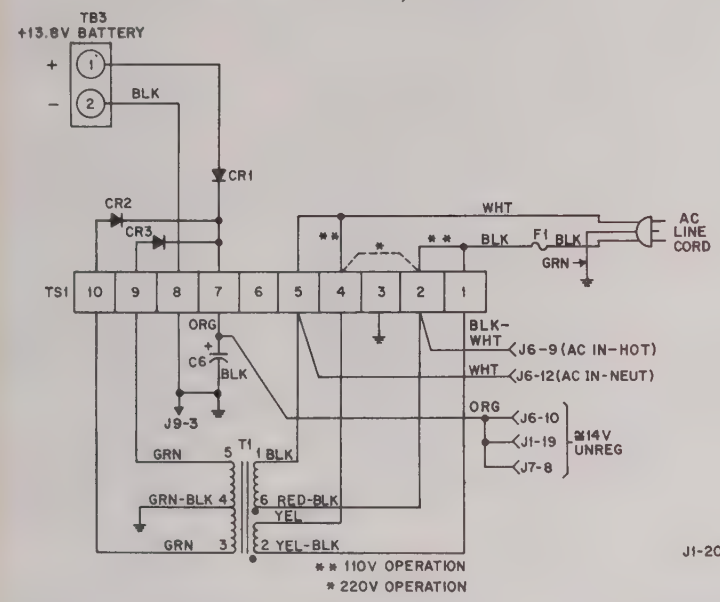
Breaks in the printed circuit wiring can be repaired by bridging the gap with solder. Remove the resin coating covering the printed wiring with solvent before soldering. Large areas of the printed wiring that have peeled loose can be repaired with a piece of hook-up wire. The hook-up wire should follow along the path of the original printed wiring. This avoids any lead dressing problem in critical circuits.

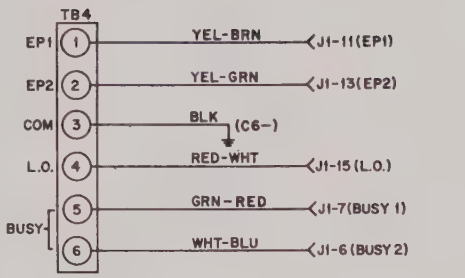
When removing resistors, capacitors and similar components, heat the connection to be loosened until the solder is molten. Then remove as much of the molten solder as possible. If the leads are bent over, use a soldering aid tool or a knife to straighten them. It may be necessary to apply the soldering iron while doing this. While applying the soldering iron, wiggle the component lightly to free it. Then lift it from the circuit board. Be sure the component leads are free before trying to remove them or you might pull loose some of the printed circuit wiring. Clean the circuit wiring around the holes with solvent. Install the new component and solder it in place. Coat the cleaned area of the circuit board with silicon resin. Such a coating seals the board from excessive moisture, prevents corrosion of the copper pattern, helps maintain insulation resistance and improves the appearance of the work. Never let solder flux bridge the gaps between the wiring pattern. This can reduce the resistance between circuits to only a few megohms which will cause leakage and disrupt certain electronic circuits. Use solvents to clean away flux after soldering. Defective components can also be replaced by clipping the leads as close to the component as possible. Solder the replacement component to these leads. Caution should be used when applying heat so that the original leads don't fall out of the board. This method of component replacement should not be used if the equipment is subjected to severe vibration.

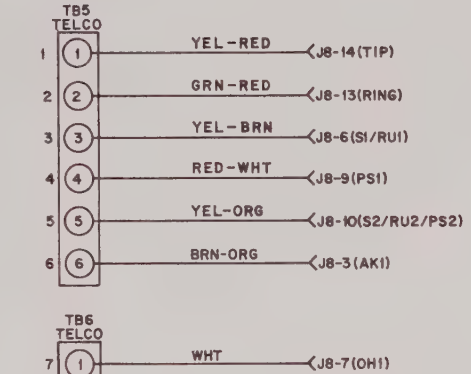
NOTES

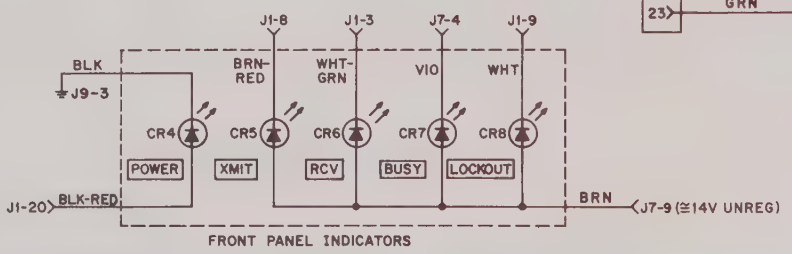


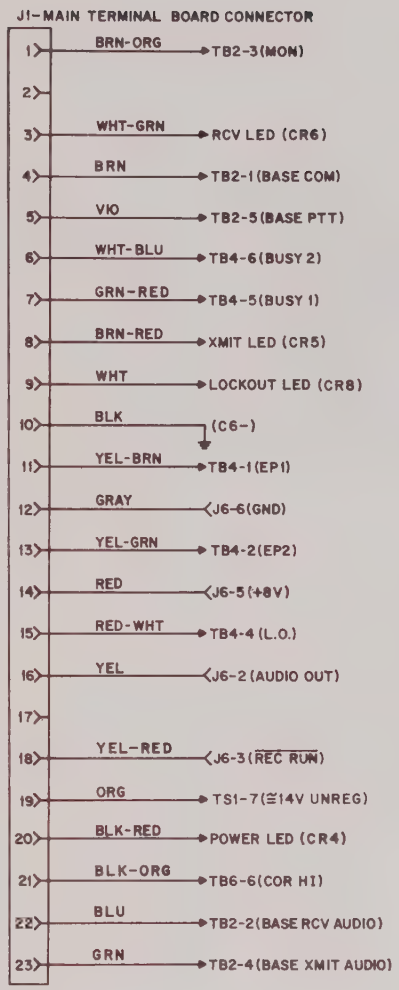


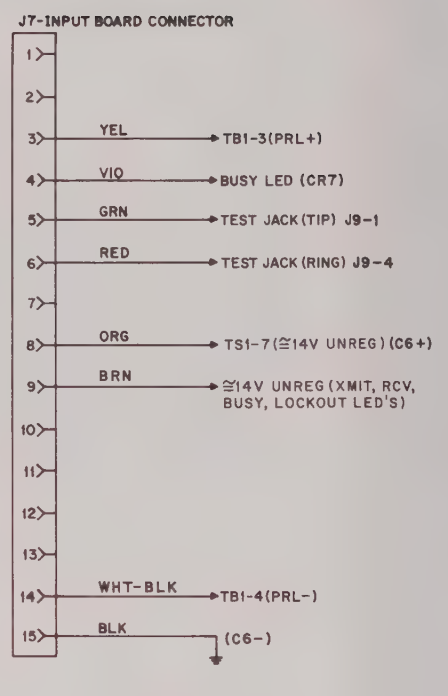


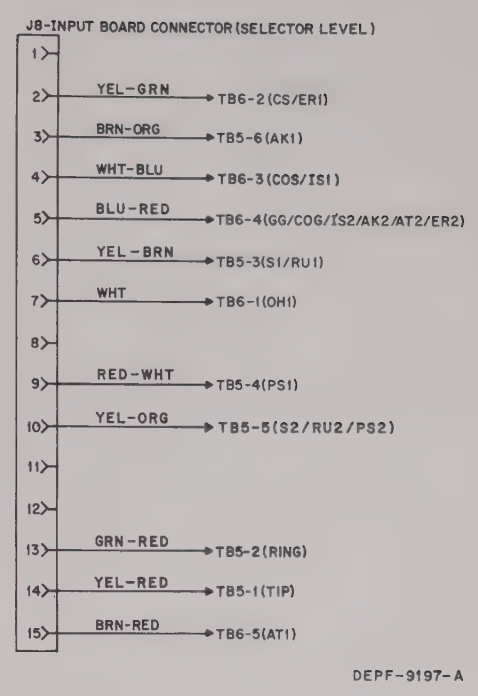












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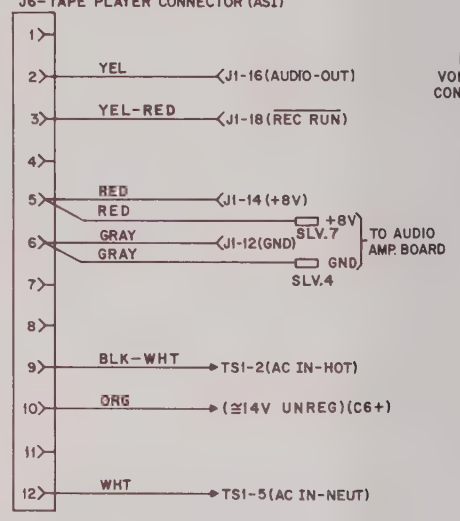
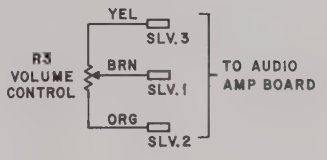




CONNECTOR INFORMATION

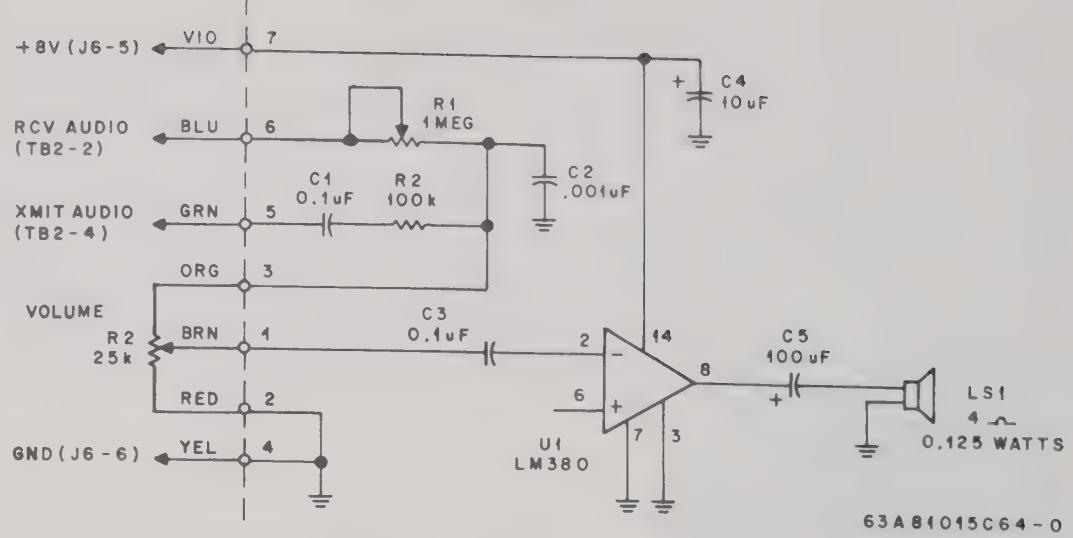
NUMBER	CONNECTS TO / FROM
J / P 1	CHASSIS / MAIN TERMINAL BOARD
J2 / P2 P2A	INPUT BOARD / UNI MAIN MAIN TERMINAL BOARD
J / P 3, 4	MAIN UNI BOARD / UNI DISPLAY BOARD
J / P 5	KEYBOARD / UNI DISPLAY BOARD
J / P 6	CHASSIS / ASI
J / P 7	CHASSIS / INPUT BOARD
P8 / J8 J8A	INPUT BOARD / CHASSIS CABLE TO J9
J9 / P9	CABLE / L.L. INTERFACE BOARD

EPF-9294-O

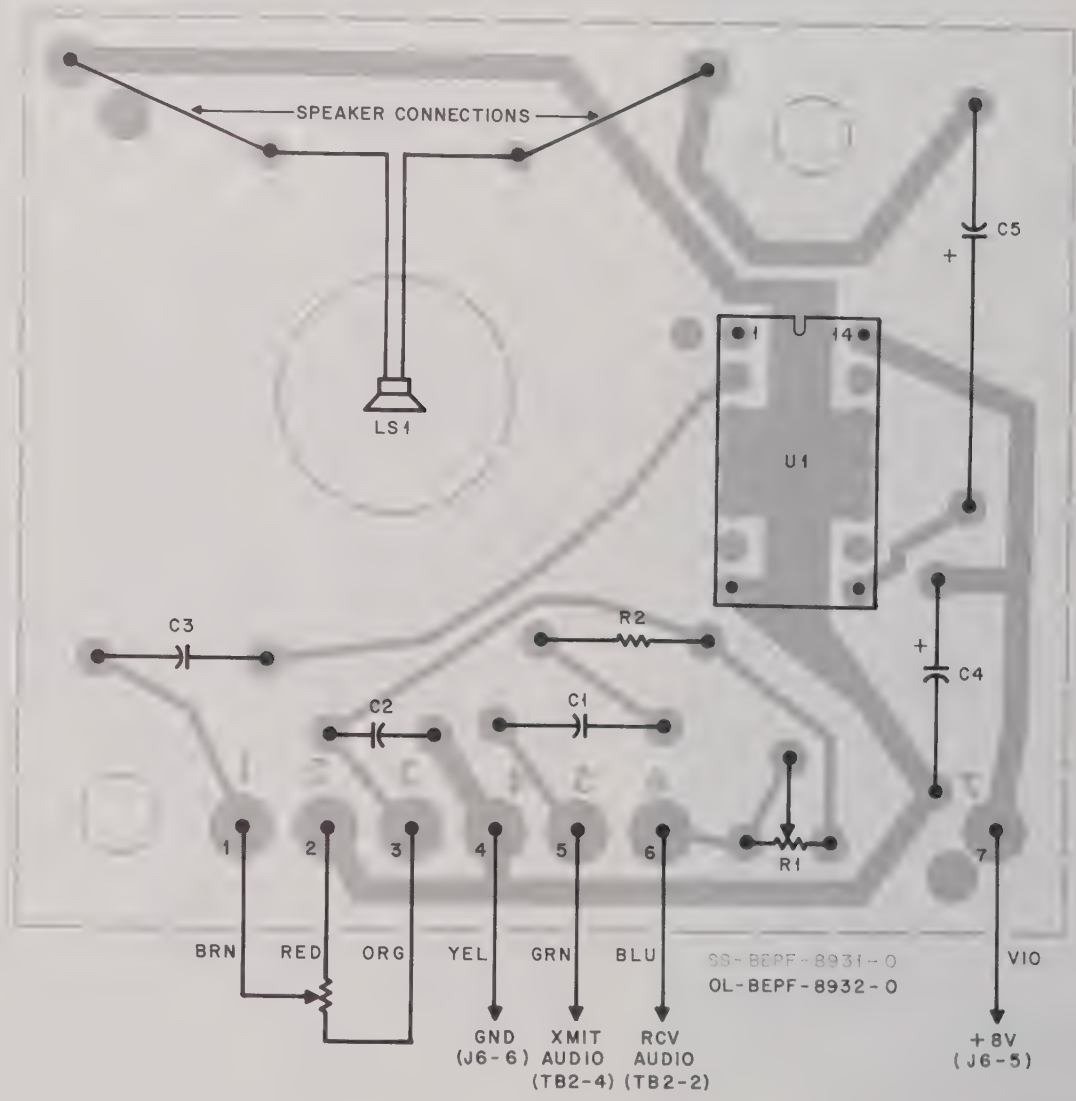
NHN6305A CHASSIS INTERCABLING AND POWER SUPPLY SCHEMATIC DIAGRAM

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		CAPACITOR, Fixed: uF ±10% 50 V unless stated
C1	0882096J18	0.1
C2	2182187B20	.001; 100 V
C3	0882096J18	0.1
C4	2384762H03	10; 20 V
C5	2382256J05	100; 10 V
C6	2383093G18	1750; 25 V
		DIODE: See Note
CR1, 2, 3	4882466H18	Rectifier, silicon
CR4 thru 8	4805174A02	LED indicator
		FUSE:
F1	6500475395	1/2 Amp.; 125 V
		JACK:
J1	0905259D20	Connector; female, 23 pins
J2, 3	0905259D01	Connector; female, 15 pins
		SPEAKER:
LS1	5082871J01	4 ohms; 300-3000 Hz
		RESISTOR, Fixed: Ω ±20%; 1/2 W
R1	1805423C93	1 Meg.
R2	0600124A97	100 k ±5%; 1/4 W
R3	1882816E08	25 k ±15%; 12 W
		SWITCH:
S1	4082372A01	Pushbutton, SPDT
		TRANSFORMER:
T1	2505247A02	Power; pri. (pin 1 BLK to pin 6 RED-BLK, 115 V input) & (pin 2 YEL-BLK to pin 7 YLK, 115 V input), (pin 8 GRAY); pin 1 to pin 2 230 V, pin 1 to pin 8 210 V, sec. (pin 3 to GRN to pin 5 GRN center tapped pin 4 GRN-YLK); 25.2 V output
		INTEGRATED CIRCUIT:
U1	5184621K33	type LM380
NONREFERENCED ITEMS		
	0200007005	NUT, hex; 6-32 x 5/16 x 7/64
	0210054A59	NUT, clip
	0200008365	NUT, Hex; 1/4-32
	0200008382	NUT, Hex; 15/32-32
	0300007229	SCREW, machine; 6-32 x 3/8
	0300007342	SCREW, machine; 6-32 x 5/8
	0300007362	SCREW, machine; 6-32 x 1/2
	0300121057	SCREW, machine; 6-32 x 3/8
	0300129071	SCREW, machine; 6-32 x 1/2
	0300135573	SCREW, tapping; 6-32 x 1/2
	0400001719	WASHER, Flat; .141 .375 .030
	0400007655	LOCKWASHER
	0400007666	LOCKWASHER
	0400007670	LOCKWASHER
	0400002642	LOCKWASHER
	0505264D01	GROMMETS
	0905426A01	PHONE, Jack
	0982083C01	RECEPTACLE, Fuse
	0983445D01	RECEPTACLE, Terminal Pin
	1405819F01	INSULATOR
	1405820F01	INSULATOR
	1482835H01	INSULATOR
	1505832F01	COVER, Top
	2705463G01	CHASSIS, Front
	2705829F01	CHASSIS, Rear
	2705830F01	CHASSIS, Bottom
	2705463G01	CHASSIS, Front
	2905260D01	TERMINALS
	2905787B02	TERMINALS
	2982336A02	TERMINALS, Female
	2983446D01	PINS, Push
	3084406H01	CORD & PLUG, AC
	3100120974	STRIP, Terminal
	3105794F02	BOARD, Terminal; 2 Lug
	3105794F03	BOARD, Terminal; 4 Lug
	3105794F04	BOARD, Terminal; 5 Lug
	3105794F05	BOARD, Terminal; 6 Lug
	3505381B02	CLOTH, Grill
	3682628H09	KNOB
	[illegible]	SLEEVE, Number 1
	3782603D02	SLEEVE, Number 2
	3782603D03	SLEEVE, Number 3
	3782603D04	SLEEVE, Number 4
	3782603D05	SLEEVE, Number 5
	3782603D06	SLEEVE, Number 6
	3782603D07	SLEEVE, Number 7
	4205565D01	CLAMP, Cable
	4205817F01	CLAMP, Cap
	4210217A02	STRAP, Tie
	4210217A19	STRAP, Tie
	4282018H12	RETAINER, Cable
	4282143C03	CLAMP, Cable
	4282999J04	RETAINER, Speaker
	4283339A04	CLAMP, Cable
	4300483437	SPACER; 1/4
	4305814F01	BUSH
	4384379C07	SPACER, Threaded
	5505475E01	KEY
	6405813F01	RECORDER, Panel
	7500864052	BUMPER, Recess
	8405425G01	BOARD, Printed Circuit

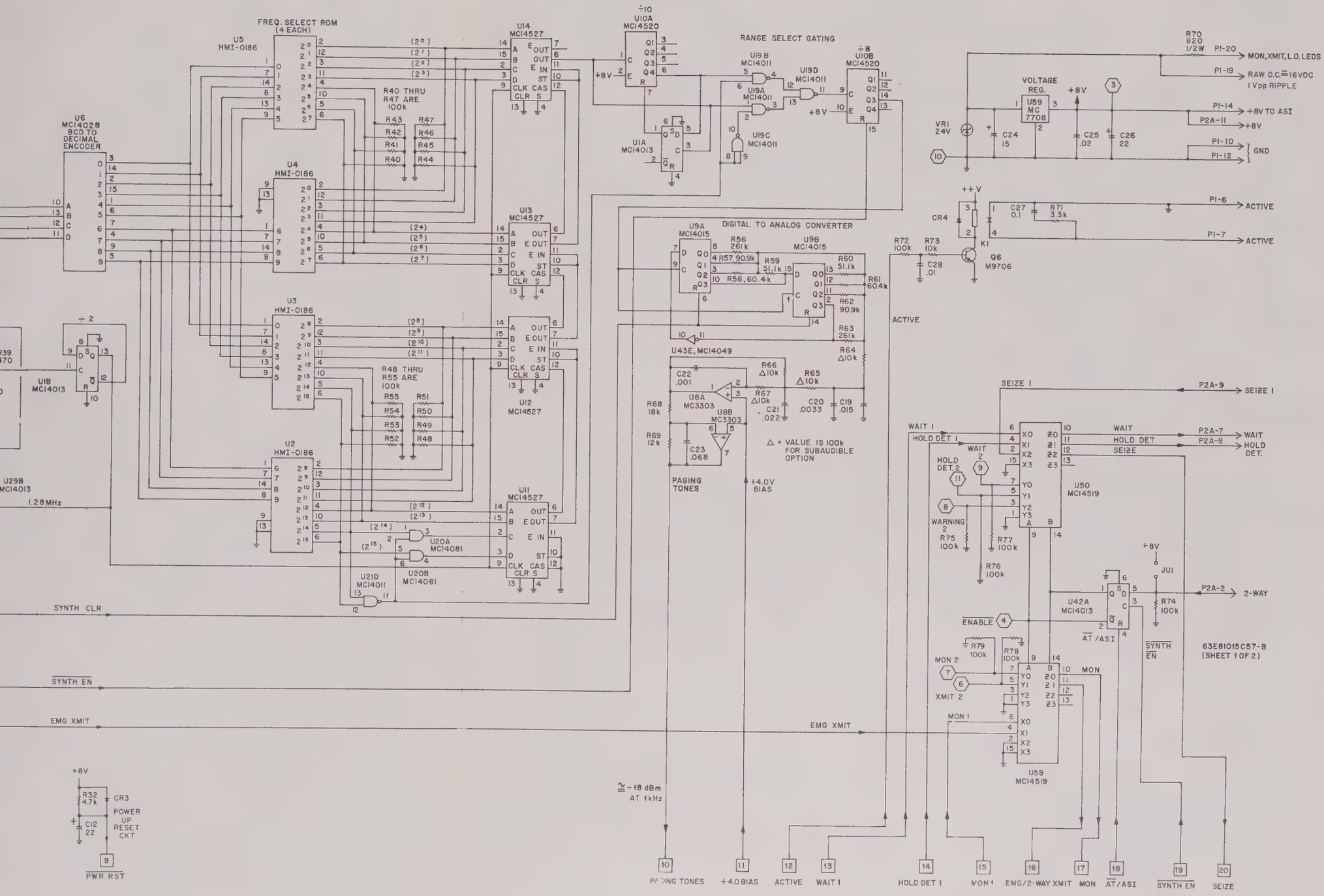
NOTE: For optimum performance, order replacement diodes by Motorola part number only.



AUDIO AMPLIFIER SCHEMATIC DIAGRAM



AUDIO AMPLIFIER CIRCUIT BOARD DETAIL


FREQ. SELECT ROM (4 EACH)
U5 HMI-0186
U4 HMI-0186
U3 HMI-0186
U2 HMI-0186
U6 MC14028 BCD TO DECIMAL ENCODER
R40 THRU R47 ARE 100k
R48 THRU R55 ARE 100k
U14 MC14527
U13 MC14527
U12 MC14527
U11 MC14527
÷10 U10A MC14520
÷8 U10B MC14520
RANGE SELECT GATING
U19B MC14011
U19D MC14011
U19A MC14011
U19C MC14011
U1A MC14013
÷2
U1B MC14013
U29B MC14013
1.28MHz
SYNTH CLR
SYNTH EN
EMG XMIT
U20A MC14081
U20B MC14081
U21D MC14011
DIGITAL TO ANALOG CONVERTER
U9A MC14015
U9B MC14015
R56 261k
R57 90.9k
R58, 60.4k
R59 51.1k
R60 51.1k
R61 60.4k
R62 90.9k
R63 261k
R64 Δ10k
R65 Δ10k
R66 Δ10k
R67 Δ10k
U43E, MC14049
U8A MC3303
U8B MC3303
C22 .001
C21 .022
C20 .0033
C19 .015
C23 .068
R68 18k
R69 12k
PAGING TONES
+4.0V BIAS
Δ = VALUE IS 100k FOR SUBAUDIBLE OPTION
ACTIVE
R72 100k
R73 10k
C28 .01
Q6 M9706
CR4
K1
++V
C27 0.1
R71 3.3k
P1-6 ACTIVE
P1-7 ACTIVE
R70 820 1/2W
P1-20 MON, XMIT, L.O. LEDS
P1-19 RAW D.C.≅16VDC 1 Vpp RIPPLE
VOLTAGE REG.
U59 MC 7708
VR1 24V
C24 15
C25 .02
C26 22
P1-14 +8V TO ASI
P2A-11 +8V
P1-10 GND
P1-12 GND
SEIZE 1
P2A-9 SEIZE 1
WAIT 1
HOLD DET 1
WAIT 2
HOLD DET 2
WARNING 2
R75 100k
R76 100k
R77 100k
U50 MC14519
P2A-7 WAIT
P2A-8 HOLD DET.
SEIZE
JU1
U42A MC14013
R74 100k
P2A-2 2-WAY
ENABLE
AT/ASI
SYNTH EN
R79 100k
R78 100k
MON 2
XMIT 2
MON 1
MON
U58 MC14519
≅ -18 dBm AT 1kHz
+8V
R32 4.7k
CR3
C12 22
POWER UP RESET CKT
PWR RST
63E81015C57-B (SHEET 1 OF 2)
10 PAGING TONES
11 +4.0 BIAS
12 ACTIVE
13 WAIT 1
14 HOLD DET 1
15 MON 1
16 EMG/2-WAY XMIT
17 MON
18 AT/ASI
19 SYNTH EN
20 SEIZE

NOTES

INTEGRATED CIRCUIT VOLTAGE
& GROUND PIN DESIGNATIONS

REF. DES.	TYPE NUMBER	+8V	GND
U1, 29, 30, 42, 45, 54, 56	MC14013	14	7
U2 THRU U5	HM1-0186	–	–
U6	MC14028	16	8
U7, 15, 16, 25, 26, 50, 58	MC14519	16	8
U8, 51	MC3303	4	11
U9	MC14015	16	8
U10	MC14520	16	8
U11 THRU U14	MC14527	16	8
U17, 18, 32, 39, 41, 47, 53	NE556	14	7
U19, 21, 36, 46	MC14011	14	7
U20, 35, 48	MC14081	14	7
U22, 37, 52, 55, 57	MC14001	14	7
U23	MC14002	14	7
U24	MC14507	14	7
U27, 34	MC14016	14	7
U28	MC14075	14	7
U31, 44	MC14071	14	7
U33, 43, 49	MC14069	14	7
U38	MC14572	16	8
U40	MC14024	14	7
U59	MC7708	–	–
U60, 61, 62	M2134 (4N27)	–	–

EPF-8771-O

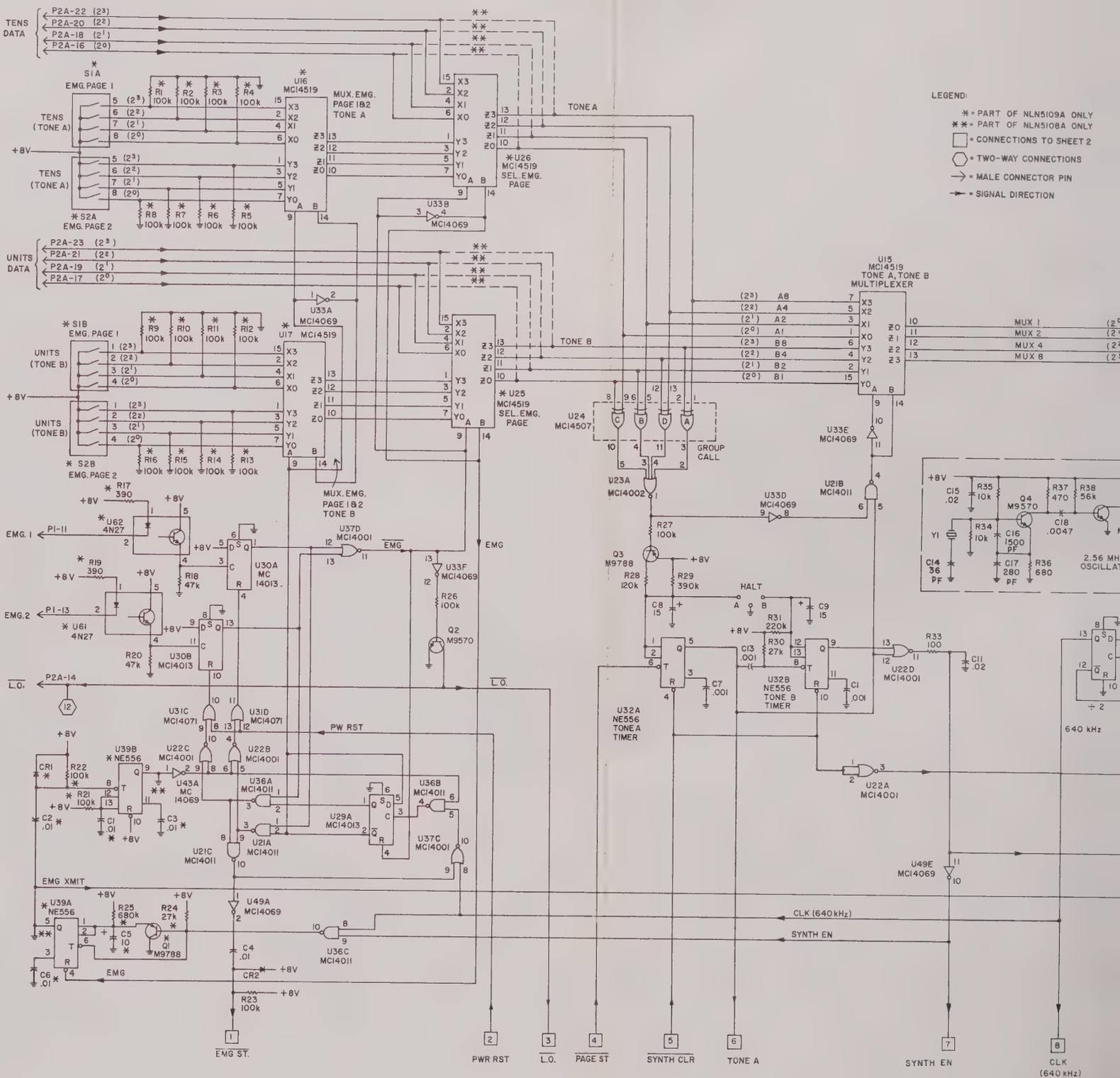
NOTES: UNLESS OTHERWISE STATED:
RESISTOR VALUES ARE IN OHMS, k = 1000;
CAPACITOR VALUES ARE IN MICROFARADS (uF);
INDUCTOR VALUES ARE IN HENRYS (H).

EPF-7506-O

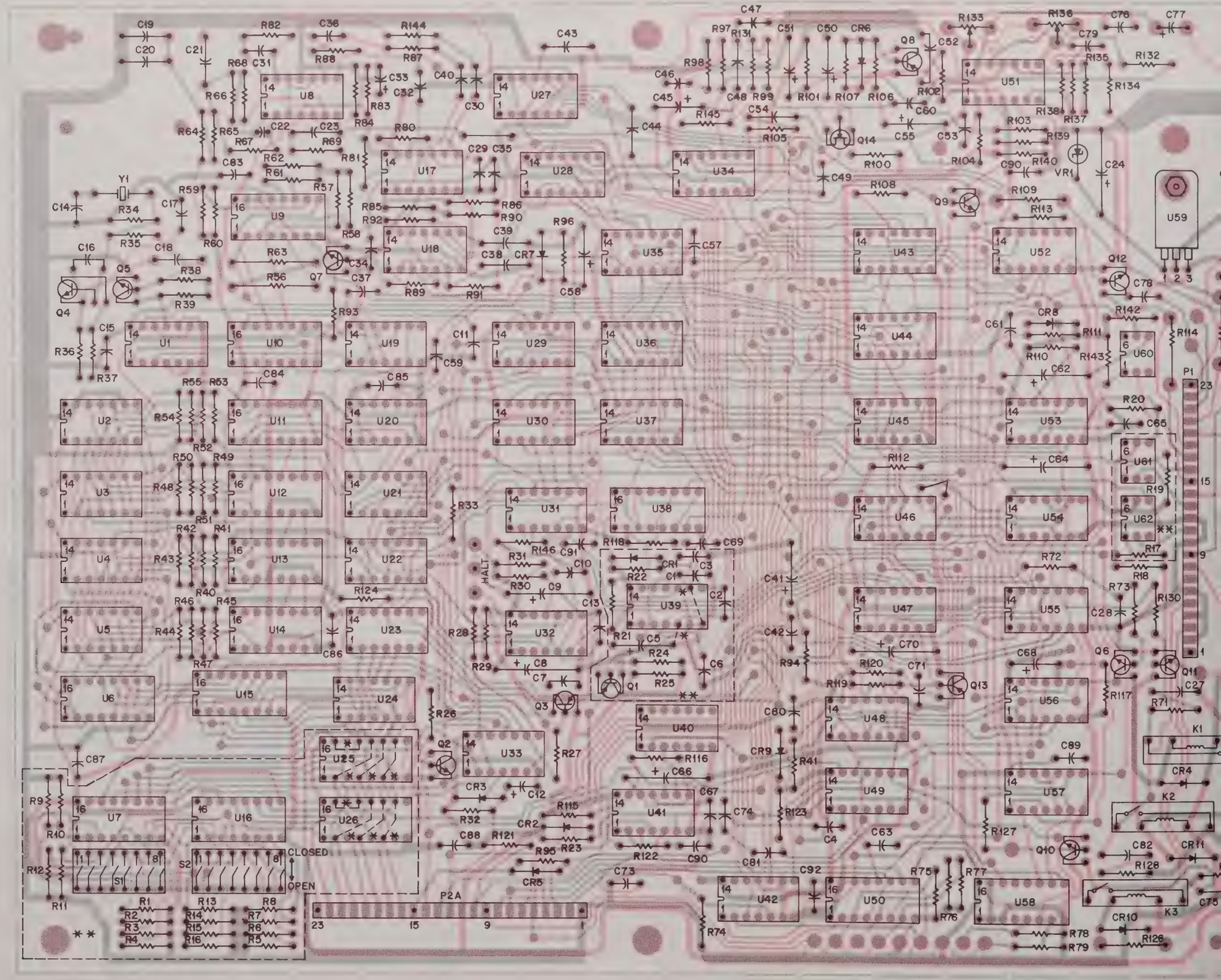
CONNECTOR INFORMATION

NUMBER	CONNECTS TO / FROM
J / P 1	CHASSIS / MAIN TERMINAL BOARD
J2 / P2 P2A	INPUT BOARD / UNI MAIN MAIN TERMINAL BOARD
J / P 3, 4	MAIN UNI BOARD / UNI DISPLAY BOARD
J / P 5	KEYBOARD / UNI DISPLAY BOARD
J / P 6	CHASSIS / ASI
J / P 7	CHASSIS / INPUT BOARD
P8 / J8 J8A	INPUT BOARD / CHASSIS CABLE TO J9
J9 / P9	CABLE / L.L. INTERFACE BOARD

EPF-9294-O



VIEWED FROM COMPONENT SIDE



* = JUMPERS (10) ADDED FOR NLN5108A KIT

** = COMPONENTS IN OUTLINED AREAS DELETED FOR NLN5108A KIT.

SS-DEPF
CS-DEPF
OL-DEPF

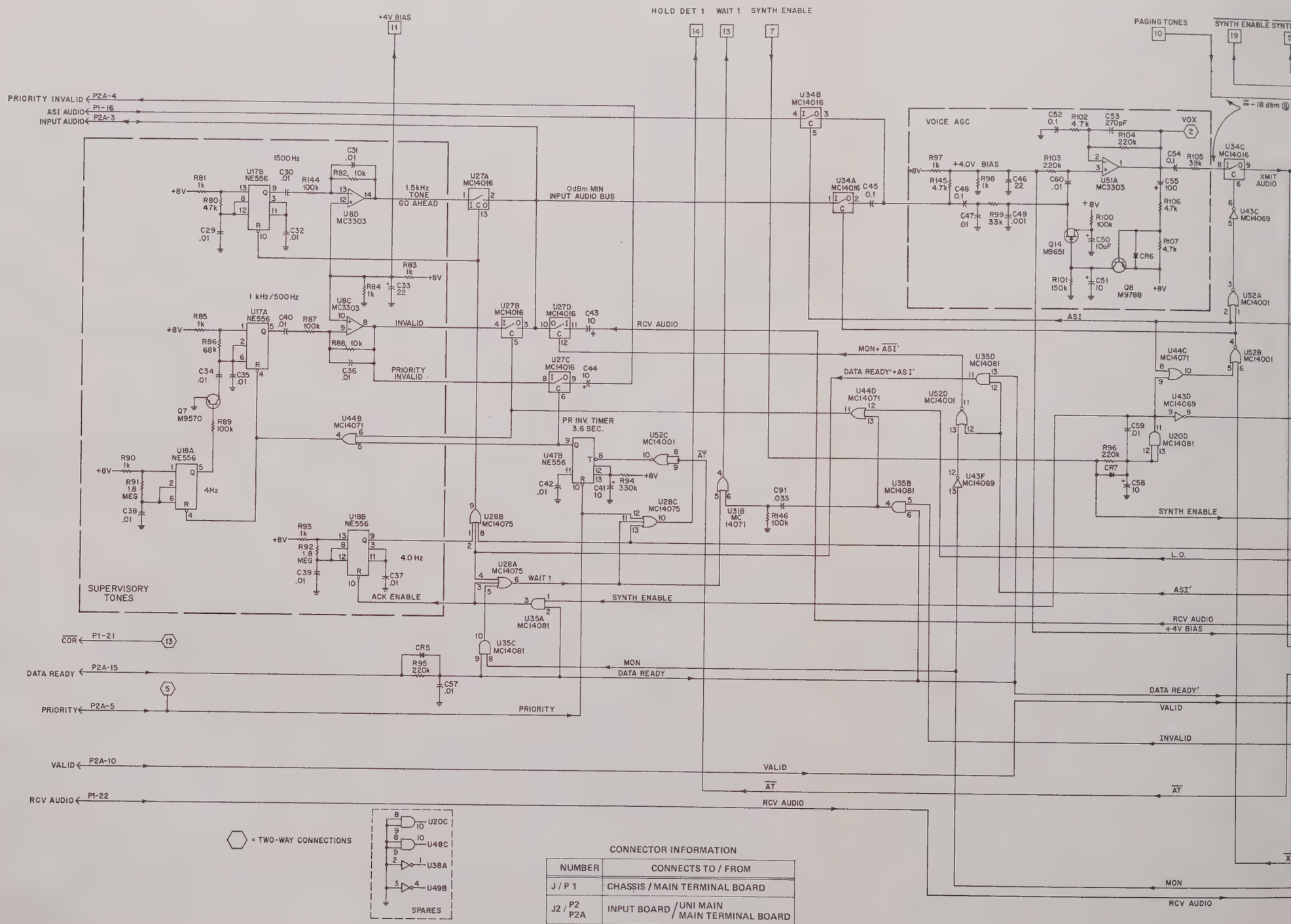
MAIN TERMINAL CIRCUIT BOARD DETAIL

NLN5108A Main Circuit Board
NLN5109A Main Circuit Board with Emergency Page PLF-1449-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		CAPACITOR, Fixed: uF ±10%; 100 V unless stated
C1, 2, 3	2182428B21	.01 -30+10% (NLN5109A only)
C4	2182428B21	.01 -30+10%
C5	2384762H03	10; 20 V (NLN5109A only)
C6	2182428B21	.01 -30+10% (NLN5109A only)
C7	2182187B20	.001
C8, 9	2382783B24	15; 25 V
C10	2182187B20	.001
C11	2182428B18	.02 -40+60%
C12	2383441B28	22 uF ±20%; 15 V
C13	2182187B20	.001
C14	2184426B16	36 pF ±5%; 500 V
C15	2182428B18	.02 -40+60%
C16	2184426B63	1500 pF ±5%
C17	2184426B54	280 pF ±5%; 500 V
C18	0882905G26	.0047
C19	0882905G10	.015; 50 V
C20	0882905G25	.0033
C21	0882905G02	.022; 50 V
C22	2182213E08	1000 pF ±5%
C23	0882905G04	.068
C24	2382783B24	15; 25 V
C25	2182428B18	.02 -40+60%
C26	2383214C07	22 ±20%; 15 V
C27	0882096J18	0.1; 250 V
C28 thru 32	2182428B21	.01 -30+10%
C33	2383441B28	22 ±20%; 15 V
C34 thru 37	2182428B21	.01 -30+10%
C38, 39	0882096J18	0.1; 250 V
C40	2182428B21	.01 -30+10%
C41	2384762H03	10; 20 V
C42	2182428B21	.01 -30+10%
C43, 44	2384762H03	10; 20 V
C45	0882096J18	0.1; 250 V
C46	2383441B28	22 ±20%; 15 V
C47	2182428B21	.01 -30+10%
C48	0882096J18	0.1; 250 V
C49	2182187B20	.001
C50, 51	2384762H03	10; 20 V
C52	0882096J18	0.1; 250 V
C53	2184494B14	270 pF ±5%; 500 V
C54	0882096J18	0.1; 150 V
C55	2384762H03	10; 20 V
C56	Not Used	
C57	2182428B21	.01 -30+10%
C58	2384762H03	10; 20 V
C59, 60, 61	2182428B21	.01 -30+10%
C62	2382783B24	15; 25 V
C63	2182428B21	.01 -30+10%
C64	2382783B24	15; 25 V
C65	2182428B21	.01 -30+10%
C66	2382783B24	15; 25 V
C67	2182428B21	.01 -30+10%
C68	2382783B14	1; 15 V
C69	2182187B20	.001
C70	2382783B24	15; 25 V
C71, 72, 73	2182428B21	.01 -30+10%
C74	2182187B20	.001
C75	0882096J18	0.1; 250 V
C76	2182187B20	.001
C77	2383441B32	47 ±20%; 20 V
C78	2184008H21	.15
C79	2182428B21	.01 -30+10%
C81	2182428B21	.01 -30+10%
C82	0882096J18	0.1; 250 V
C83 thru 90	2182428B21	.01 -30+10%
C91	2184008H06	.033; 50 V
C92	2182428B21	.01 -30+10%
		DIODE: See Note I
CR1	4883654H01	Silicon (NLN5109A only)
CR2 thru 11	4883654H01	Silicon
		RELAY:
K1, 2, 3	8005103G01	Reed type
		PLUG:
P1, 2A	0905818F03	Connector, male; 23-pin
		TRANSISTOR: See Note I
Q1	4800869788	PNP; type M9788
Q2	4800869570	NPN; type M9570
Q3	4800869788	PNP; type M9788
Q4, 5	4800869570	NPN; type M9570
Q6	4800869706	NPN; type M9706
Q7	4880869570	NPN; type M9570
Q8	4800869788	PNP; type M9788
Q9	4800869570	NPN; type M9570
Q10, 11, 12	4800869706	NPN; type M9706
Q13	4880869788	PNP; type M9788
Q14	4880869651	FET; type M9651
		RESISTOR, Fixed: Ω ±5%; 1/4 W unless stated
R1 thru 16	0600124A97	100 k (NLN5109A only)
R17	0600124A39	390 (NLN5109A only)
R18	0600124A89	47 k
R19	0600124A39	390 (NLN5109A only)
R20	0600124A89	47 k
R21	0600124A97	100 k (NLN5109A only)
R22, 23	0600124A97	100 k
R24	0600124A83	27 k (NLN5109A only)
R25	0600124B18	680 k (NLN5109A only)
R26, 27	0600124A97	100 k
R28	0600124A99	120 k
R29	0600124B12	390 k
R30	0600124A83	27 k
R31	0600124B06	220 k
R32	0600124A65	4.7 k
R33	0600124A25	100
R34, 35	0600124A73	10 k
R36	0600124C45	680
R37	0600124C41	470
R38	0600124C91	56 k
R39	0600124C41	470
R40 thru 55	0600124A97	100 k
R56	0683175B99	261 k ±1%
R57	0683175C76	90.9 k ±1%
R58	0683175C64	60.4 k ±1%
R59, 60	0683175C60	51.1 k ±1%
R61	0683175C64	60.4 k ±1%
R62	0683175C76	90.9 k ±1%
R63	0683175B99	261 k ±1%
R64 thru 67	0600124A73	10 k
R68	0600124A79	18 k
R69	0600124C75	12 k
R70	0600125A47	820; 1/2 W
R71	0600124A61	3.3 k
R72	0600124A97	100 k
R73	0600124A73	10 k
R74 thru 79	0600124A97	100 k
R80	0600124A89	47 k
R81	0600124A49	1 k
R82	0600124A73	10 k
R83, 84, 85	0600124A49	1 k
R86	0600124A93	68 k
R87	0600124A97	100 k
R88	0600124A73	10 k
R89	0600124A97	100 k
R90	0600124A49	1 k
R91, 92	0600124B28	1.8 Meg.
R93	0600124A49	1 k
R94	0600124B10	330 k
R95, 96	0600124B06	220 k
R97, 98	0600124A49	1 k
R99	0600124A85	33 k
R100	0600124A97	100 k
R101	0600124B02	150 k
R102	0600124A65	4.7 k
R103, 104	0600124B06	220 k
R105	0600124A87	39 k
R106, 107	0600124A65	4.7 k
R108	0600124A85	33 k
R109	0600125A47	820; 1/2 W
R110	0600124A85	33 k
R111	0600124A97	100 k
R112	0600124B22	1 Meg.
R113	0600124A97	100 k
R114	0600125A47	820; 1/2 W
R115	0600124A49	1 k
R116	0600124B16	560 k
R117, 118	0600124A97	100 k
R119	0600124A83	27 k
R120	0600124B04	180 k
R121 thru 124	0600124A97	100 k
R125	0600124A61	3.3 k
R126	0600125A47	820; 1/2 W
R127	0600124A97	100 k
R128	0600124A61	3.3 k
R129	0600125A47	820; 1/2 W
R130	0600124A97	100 k
R131, 132	0600124A65	4.7 k
R133	1883083G26	Pot., 50 k
R134	0660124A73	10 k
R135	0600124A89	47 k
R136	1883083G26	Pot., 50 k
R137, 138, 139	0600124A73	10 k
R140	0600124A59	2.7 k
R141	0600124A97	100 k
R142	0600124A83	27 k
R143	0600124A39	390
R144	0600124A97	100 k
R145	0600124A65	4.7 k
R146	0600124A97	100 k
		SWITCH:
S1, 2	4083849F02	8-position (NLN5109A only)
		INTEGRATED CIRCUIT: See Note I
U1	5184887K13	CMOS; type MC14013
U2 thru 5	---------	Factory programmed Read-Only Memory (See Note II)
U6	5184887K20	CMOS; type MC14028
U7	5182822F28	CMOS; type 14519 (NLN5109A only)
U8	5184621K32	type MC3303
U9	5182822F11	CMOS; type MC14015
U10	5182822F34	CMOS; type MC14520
U11 thru 14	5182822F52	CMOS; type MC14527
U15	5182822F28	CMOS; type MC14519
U16	5182822F28	CMOS; type MC14519 (NLN5109A only)
U17, 18	5184320A85	type NE556
U19	5184887K08	CMOS; type MC14011
U20	5182822F44	CMOS; type MC14081
U21	5184887K08	CMOS; type MC14011
U22	5184887K09	CMOS; type MC14001
U23	5184887K37	type MC14002
U24	5182822F18	CMOS; type MC14507
U25, 26	5182822F28	CMOS; type MC14519 (NLN5109A only)
U27	5184887K04	CMOS; type MC14016
U28	5184887K29	type MC14075
U29, 30	5184887K13	CMOS; type MC14013
U31	5182822F43	CMOS; type MC14071
U32	5184320A85	type NE556
U33	5184887K11	CMOS; type 14069
U34	5184887K04	CMOS; type MC14016
U35	5182822F44	CMOS; type MC14081
U36	5184887K08	CMOS; type MC14011
U37	5184887K09	CMOS; type MC14001
U38	5182822F48	CMOS; type MC14572
U39	5184320A85	type NE556 (NLN5109A only)
U40	5184887K34	CMOS; type MC14024
U41	5184320A85	type NE556
U42	5184887K13	CMOS; type MC14013
U43	5184887K11	CMOS; type MC14069
U44	5182822F43	CMOS; type MC14071
U45	5184887K13	CMOS; type MC14013
U46	5184887K08	CMOS; type MC14011
U47	5184320A85	type NE556
U48	5182822F44	CMOS; type MC14081
U49	5184887K11	CMOS; type MC14069
U50	5182822F28	CMOS; type MC14519
U51	5184621K32	type MC3303
U52	5184887K09	CMOS; type MC14001
U53	5184320A85	type NE556
U54	5184887K13	CMOS; type MC14013
U55	5184887K09	CMOS; type MC14001
U56	5184887K13	CMOS; type MC14013
U57	5184887K09	CMOS; type MC14001
U58	5182822F28	CMOS; type MC14519
U59	5184621K16	type MC7708
U60, 61	5184621K34	type M2134
U62	5184621K34	type M2134 (NLN5109A only)
		DIODE: See Note I
VR1	4883461E11	Zener, 24 V
		CRYSTAL: See Note III
Y1	4805386E01	Resonator

NONREFERENCED ITEMS		
	0200007019	NUT, Hex; 4-40 x 1/4" x 3/32"
	0300001930	SCREW, Slotted; 4-40 x 3/8"
	0400007667	LOCKWASHER, #4
	0905388E01	SOCKET (for U2 thru 5)
	0983445001	RECEPTACLE, Pin
	2605816F01	HEAT SINK
	8405905F01	CIRCUIT BOARD

NOTES:
I. For optimum performance, order replacement diodes, transistors, and integrated circuits by Motorola part number only.
II. When ordering ROM's, specify ROM kit number NLN1442A, and specify tone group to be programmed.
III. When ordering crystal units, specify operating frequency, crystal frequency, and part number (type).



CONNECTOR INFORMATION

NUMBER	CONNECTS TO / FROM
J / P 1	CHASSIS / MAIN TERMINAL BOARD
J2 / P2 P2A	INPUT BOARD / UNI MAIN MAIN TERMINAL BOARD
J / P 3, 4	MAIN UNI BOARD / UNI DISPLAY BOARD
J / P 5	KEYBOARD / UNI DISPLAY BOARD
J / P 6	CHASSIS / ASI
J / P 7	CHASSIS / INPUT BOARD
P8 / J8 J8A	INPUT BOARD / CHASSIS CABLE TO J9
J9 / P9	CABLE / L.L. INTERFACE BOARD

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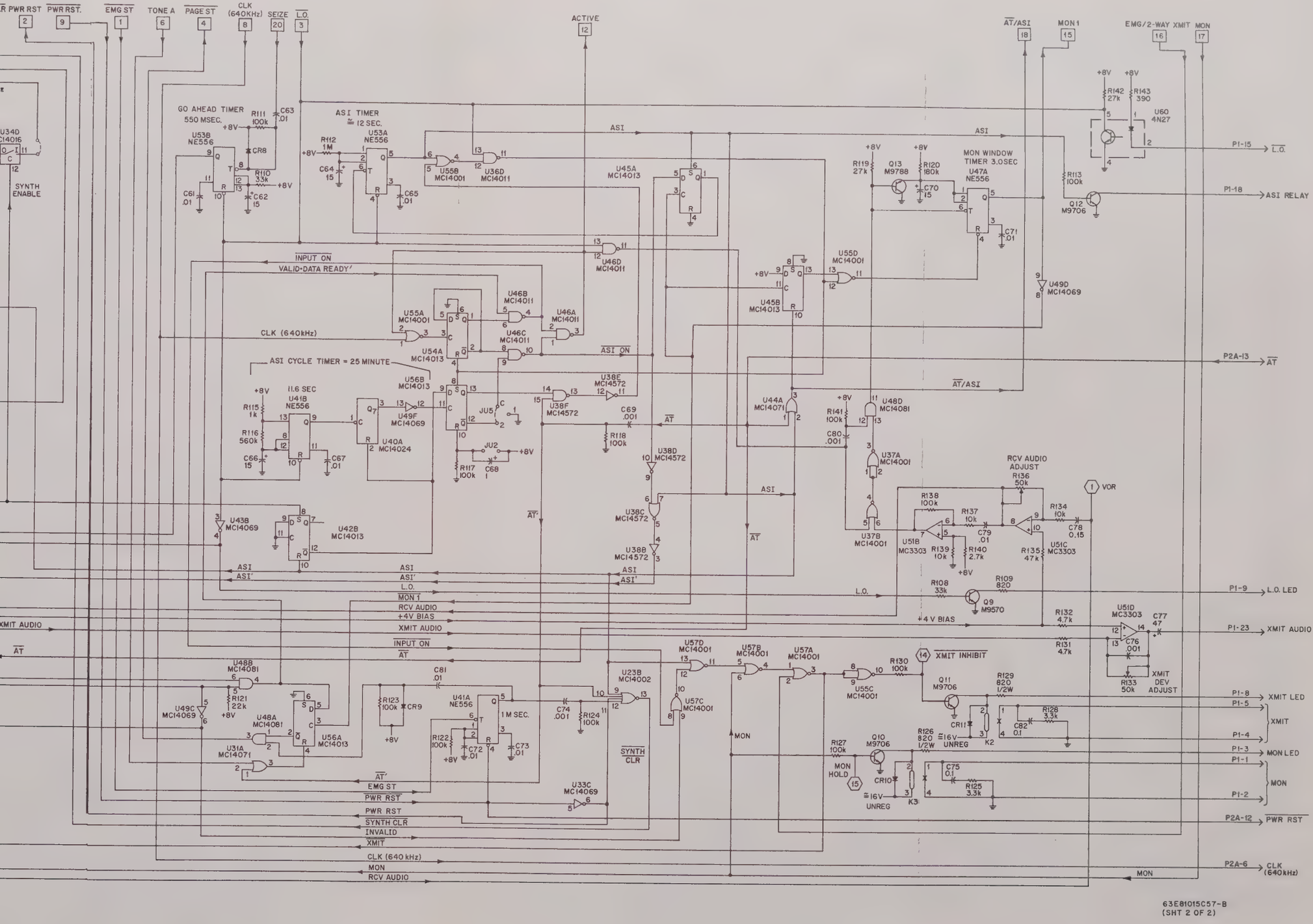
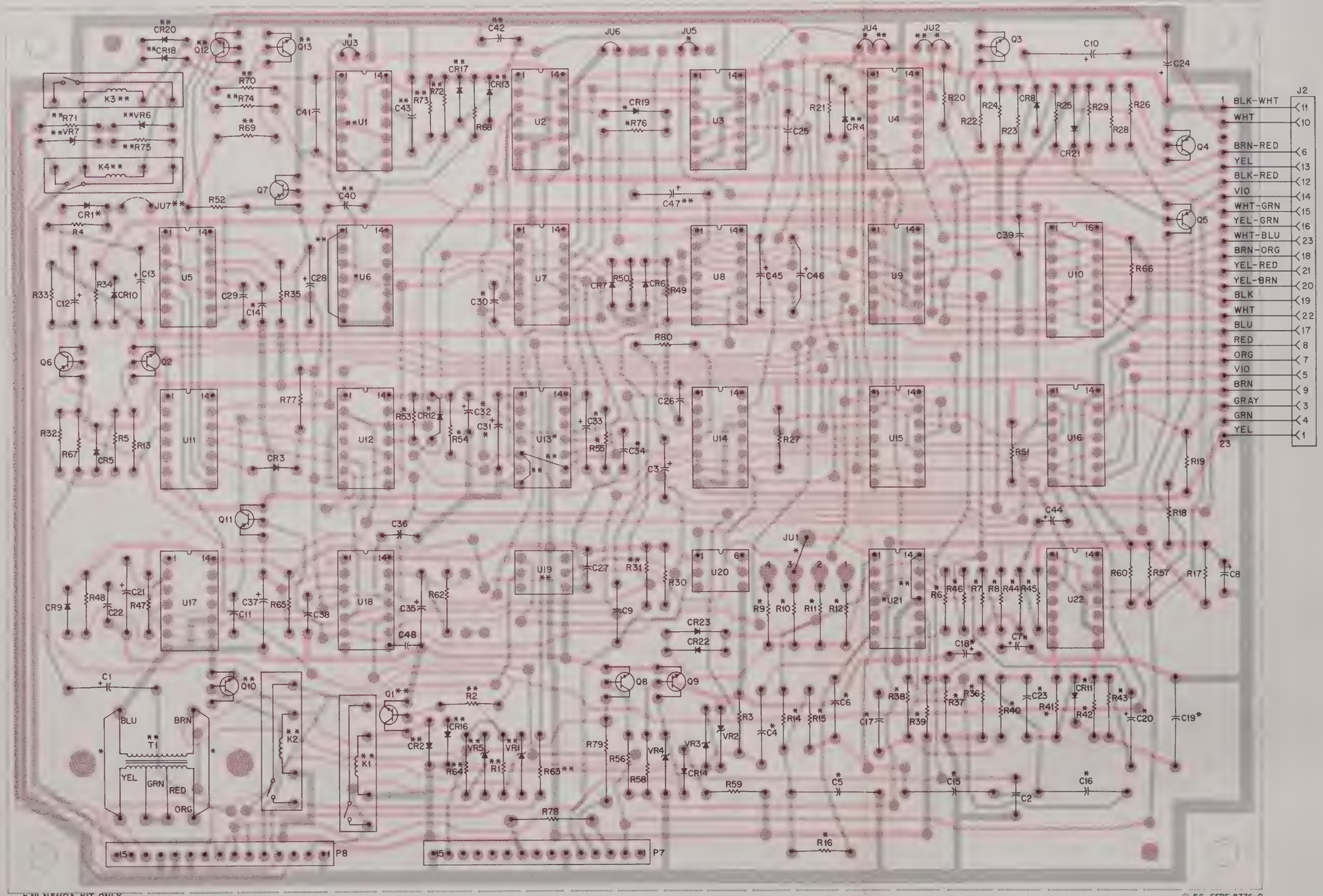


63E81015C57-B
(SHT 2 OF 2)

MAIN TERMINAL BOARD
SCHEMATIC DIAGRAM (2 of 2)

VIEWED FROM COMPONENT SIDE



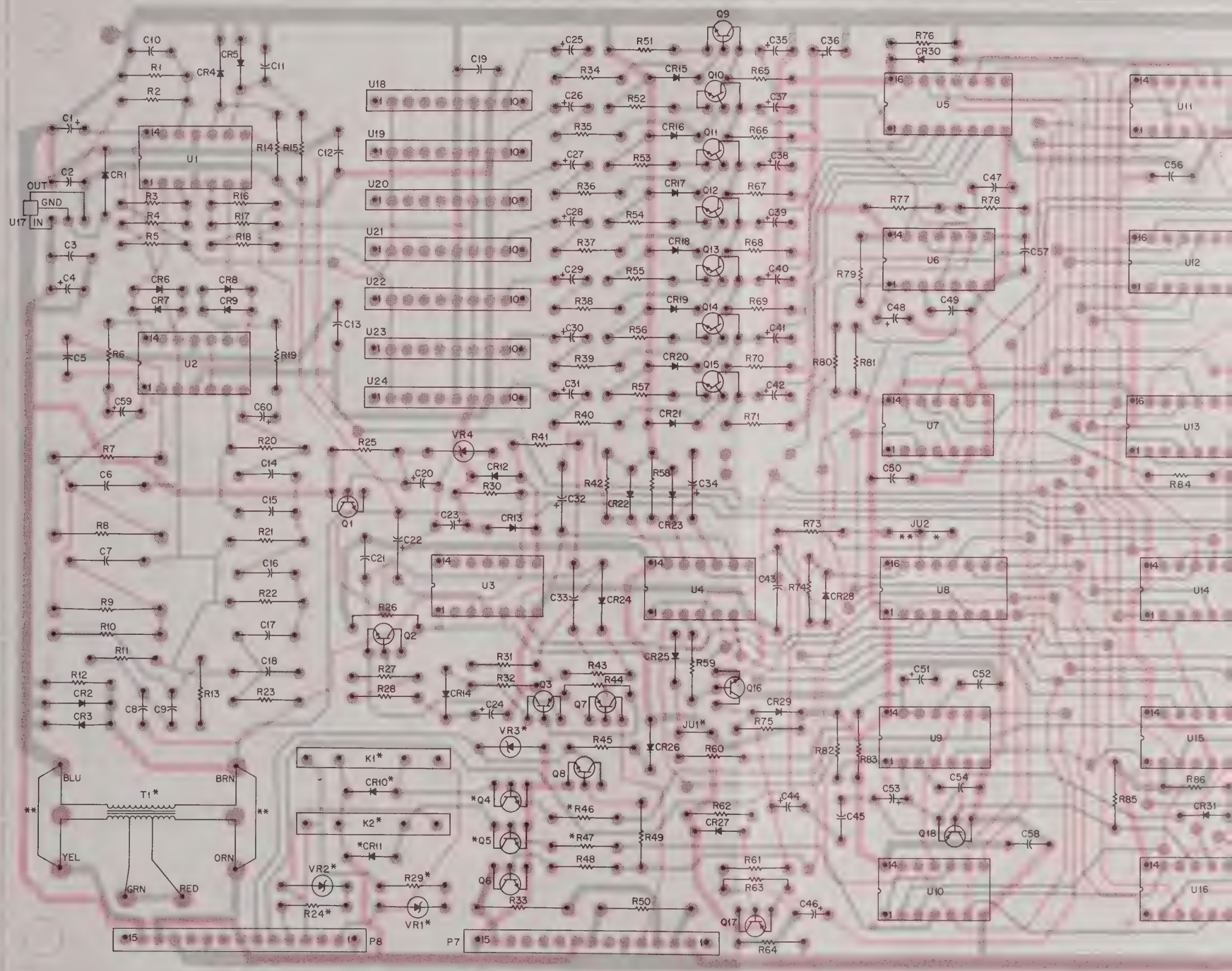
* NLN5110A KIT ONLY.
** NLN5111A KIT ONLY.

SS EEPF-8776-O
CS EEPF-8777-O
OL EEPF-8778-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		CAPACITOR, Fixed: uF ±10%; 20 V unless stated
C1	2384762H03	10
C2	2182428B21	.01 -30+10%; 100 V
C3	2384762H03	10
C4	2384762H03	10 (NLN5110A only)
C5	0882096J20	0.22; 250 V (NLN5110A only)
C6	0882905G08	.033; 50 V (NLN5110A only)
C7	2383441B28	22 ±20%; 15 V (NLN5110A only)
C8	2383441B28	22 ±20%; 15 V
C9	0882096J18	0.1; 50 V
C10	2382256J06	2.2; 63 V
C11	2182428B21	.01 -30+10%; 100 V
C12, 13	2384762H03	10
C14	2182428B21	.01 -30+10%; 100 V
C15, 16	0882096J20	0.22; 250 V (NLN5110A only)
C17	0882096J18	0.1; 50 V (NLN5110A only)
C18	2383441B28	22 ±20%; 15 V (NLN5110A only)
C19	0882096J20	0.22; 250 V (NLN5110A only)
C20	2384762H03	10 (NLN5110A only)
C21	2382783B14	1; 15 V
C22	2182428B21	.01 -30+10%; 100 V
C23	0882096J18	0.1; 50 V (NLN5110A only)
C24	2384762H03	10
C25, 26, 27	2182428B21	.01 -30+10%; 100 V
C28	2384762H03	10
C29	2182428B21	.01 -30+10%; 100 V
C30	2182428B21	.01 -30+10%; 100 V (NLN5110A only)
C31	2382783B14	1; 15 V (NLN5110A only)
C32	2182428B21	.01 -30+10% (NLN5110A only)
C33	2382783B14	1; 15 V (NLN5110A only)
C34	2182428B21	.01 -30+10% (NLN5110A only)
C35	2384762H03	10
C36	2182428B21	.01 -30+10%
C37	2384762H03	10
C38, 39	2182428B21	.01 -30+10%
C40	2182428B21	.01 -30+10% (NLN5111A only)
C41	2382783B14	1; 15 V (NLN5111A only)
C42	2182428B21	.01 -30+10%
C43	2382783B14	1; 15 V (NLN5111A only)
C44	2383441B28	22 ±20%; 15 V (NLN5110A only)
C45, 46	2382783B14	1; 15 V
C47	2384762H05	4.7 ±20% (NLN5111A only)
C48	2184008H01	.01 ±10%; 50 V
		DIODE: See Note
CR1	4883654H01	Silicon (NLN5110A only)
CR2	4883654H01	Silicon (NLN5111A only)
CR3	4883654H01	Silicon
CR4	4883654H01	Silicon (NLN5111A only)
CR5 thru 10	4883654H01	Silicon
CR11, 12	4883654H01	Silicon (NLN5110A only)
CR13	4883654H01	Silicon (NLN5111A only)
CR14	4883654H01	Silicon
CR15		Not Used
CR16, 17, 18	4883654H01	Silicon (NLN5111A only)
CR19	4883654H01	Silicon (NLN5110A only)
CR20	4883654H01	Silicon (NLN5111A only)
CR21	4883329G04	3-Junction
CR22, 23	4883329G04	3-Junction (NLN5110A only)
		JACK:
J2	0905259D20	Connector, Female; 23-pin
		RELAY:
K1 thru 4	8005103G01	12 V, Form A
		PLUG:
P7, 8	0905261D01	Connector, Male; 23-pin
		TRANSISTOR: See Note
Q1	4800869706	NPN; type M9706 (NLN5111A only)
Q2, 3	4800869570	NPN; type M9570
Q4, 5, 6	4800869571	PNP; type M9571
Q7	4800869788	PNP; type M9788
Q8	4800869706	NPN; type M9706
Q9	4800869572	NPN; type M9572
Q10	4800869706	PNP; type M9706 (NLN5111A only)
Q11	4800869788	PNP; type M9788
Q12, 13	4800869706	NPN; type M9706 (NLN5111A only)
		RESISTOR, Fixed: Ω ±5%; 1/4 W unless stated
R1	0600124A09	22 (NLN5111A only)
R2	0600124A97	100 k (NLN5111A only)
R3	0600124A49	1 k
R4	0600124A89	47 k
R5	0600124A81	22 k
R6	0600124A95	82 k
R7, 8	0600124A97	100 k (NLN5110A only)
R9	0600124B04	180 k (NLN5110A only)
R10	0600124A97	100 k (NLN5110A only)
R11	0600124A91	56 k (NLN5110A only)
R12	0600124A85	33 k (NLN5110A only)
R13	0600124A85	33 k
R14	0600124A69	6.8 k (NLN5110A only)
R15	0600124A75	12 k (NLN5110A only)
R16	0600124A65	4.7 k (NLN5110A only)
R17, 18	0600124A65	4.7 k
R19, 20	0600124A73	10 k
R21	0600124A77	15 k
R22	0600124A83	27 k
R23, 24	0600124A97	100 k
R25	0600124A73	10 k
R26	0600124A65	4.7 k
R27	0600124A83	27 k
R28	0600124A27	22
R29	0600124A65	4.7 k
R30	0600124A83	27 k
R31	0600124A39	390 (NLN5111A only)
R32	0600124A69	6.8 k
R33	0600124A51	1.2 k
R34	0600124A83	27 k
R35	0600124B10	330 k (NLN5110A only)
R36	0600124A71	8.2 k (NLN5110A only)
R37	0600124A97	100 k (NLN5110A only)
R38	0600124A91	56 k (NLN5110A only)
R39	0600124A97	100 k (NLN5110A only)
R40	0600124A73	10 k (NLN5110A only)
R41 thru 44	0600124A97	100 k (NLN5110A only)
R45	0600124A83	27 k (NLN5110A only)
R46	0600124B22	1 Meg. (NLN5110A only)
R47, 48	0600124A83	27 k
R49, 50	0600124A97	100 k
R51	0600124A83	27 k
R52	0600124B24	1.2 Meg.
R53	0600124A83	27 k (NLN5110A only)
R54	0600124A81	22 k (NLN5110A only)
R55	0600124A95	82 k (NLN5110A only)
R56	0600124A97	100 k
R57	0600124A83	27 k
R58	0600124A57	2.2 k
R59, 60	0600124A97	100 k
R61		Not Used
R62	0600124A81	22 k
R63	0600124A97	100 k (NLN5111A only)
R64	0600124A09	22 (NLN5111A only)
R65	0600124A79	18 k
R66	0600124A83	27 k
R67	0600124A61	3.3 k
R68	0600124A95	82 k (NLN5111A only)
R69	0600124B14	470 k
R70	0600124A97	100 k (NLN5111A only)
R71	0600124A09	22 (NLN5111A only)
R72	0600124A95	82 k (NLN5111A only)
R73	0600124B14	470 k (NLN5111A only)
R74	0600124A97	100 k (NLN5111A only)
R75	0600124A09	22 (NLN5111A only)
R76	0600124A79	18 k (NLN5110A only)
R77	0600124B12	390 k
R78, 79	0600125A47	820; 1/2 W
R80	0600124A09	22
		TRANSFORMER:
T1	2584903H01	Audio
		INTEGRATED CIRCUIT:
U1	5184320A85	type NE556 (NLN5111A only)
U2	5184887K13	CMOS; type MC14013
U3	5184887K09	CMOS; type MC14001
U4	5184887K11	CMOS; type MC14069
U5	5184320A85	type NE556
U6	5184887K13	CMOS; type MC14013 (NLN5110A only)
U7	5184887K52	type MC14584
U8	5184887K09	CMOS; type MC14001
U9	5184887K13	CMOS; type MC14013
U10	5184887K23	CMOS; type MC14518
U11	5184887K09	CMOS; type MC14001
U12	5184887K11	CMOS; type MC14069
U13	5184320A85	type NE556 (NLN5110A only)
U14	5184887K04	CMOS; type MC14016
U15, 16	5184887K09	CMOS; type MC14001
U17, 18	5184320A85	type NE556
U19	5184621K34	type M2134 (NLN5111A only)
U20	5184621K34	type M2134
U21	5184621K21	type M2121 (NLN5110A only)
U22	5184887K08	CMOS; type MC14011
		DIODE: See Note
VR1	4883461E30	53.6 V Zener (NLN5111A only)
VR2, 3	4883461E03	3.3 V Zener
VR4	4882256C58	24 V Zener
VR5, 6, 7	4883461E30	53.6 V Zener (NLN5111A only)
NONREFERENCED ITEMS		
	0200009627	NUT, Hex; #4
	0300008022	SCREW, Slotted; 4-40 x 1/4"
	0400009777	LOCKWASHER, #4
	0983445D01	RECEPTACLE, Pin
	2905260D01	TERMINAL, Single-contact
	2983446D01	TERMINAL, Pin
	4210217A02	TIE WRAP
	8405781F01	CIRCUIT BOARD

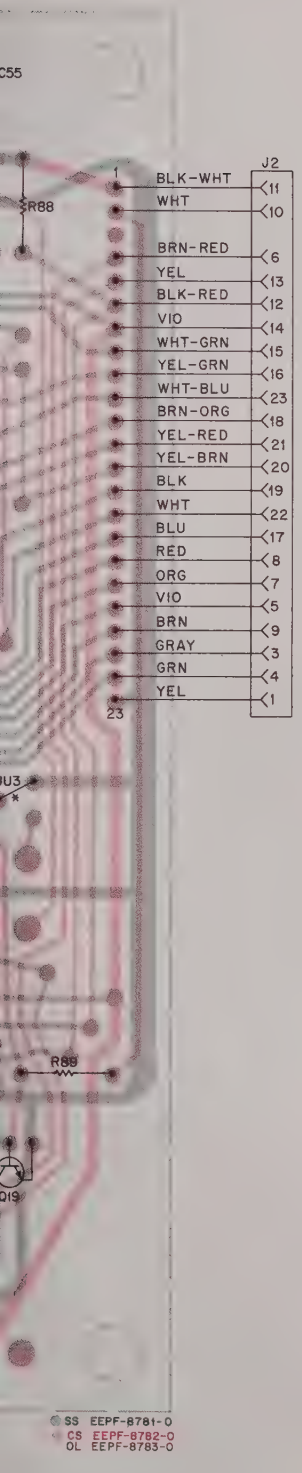
NOTE: For optimum performance, order replacement diodes, transistors, and integrated circuits by Motorola part number only.

VIEWED FROM COMPONENT SIDE



* NLN5113A KIT ONLY.

** NLN5112A KIT ONLY.

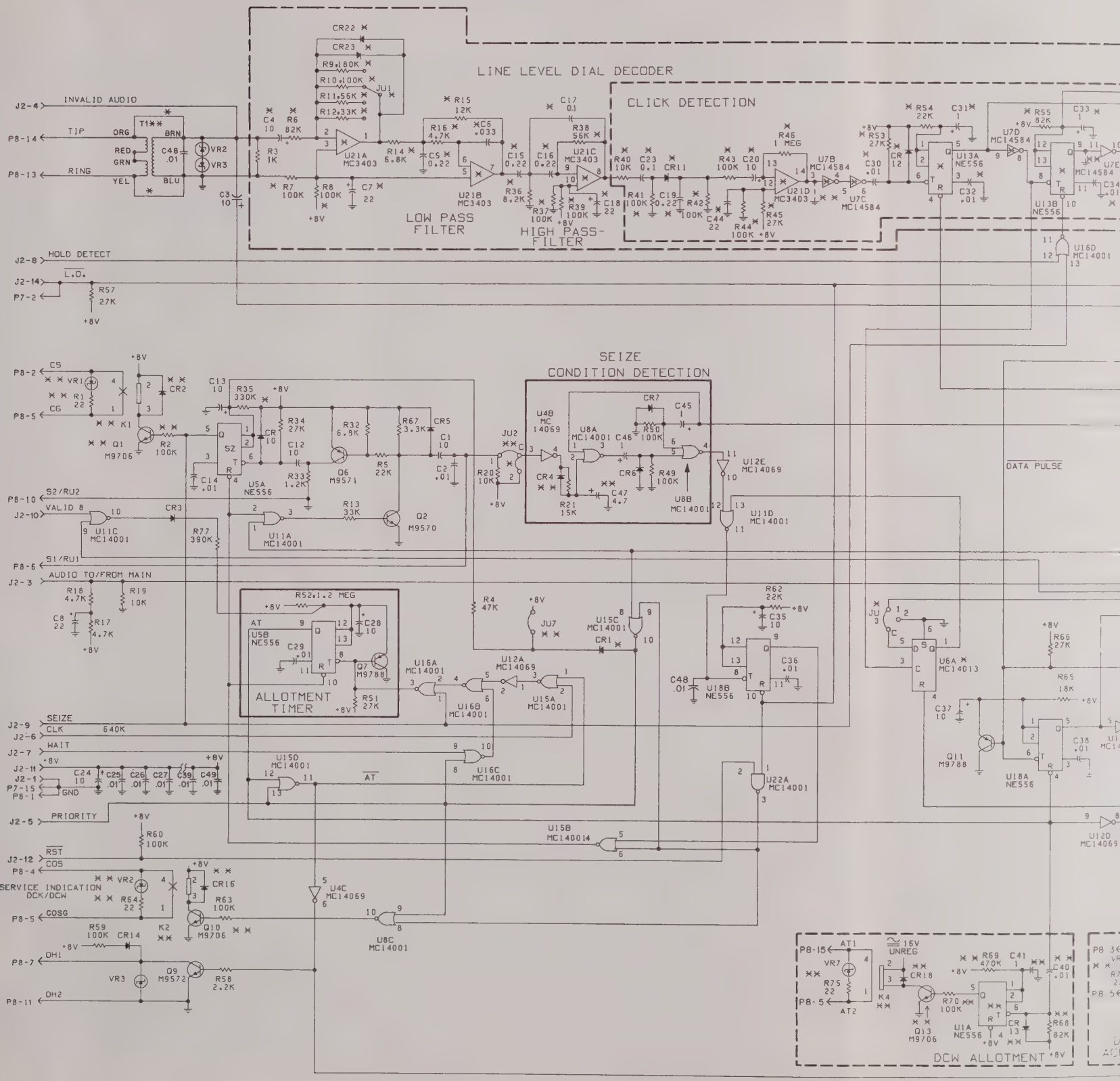


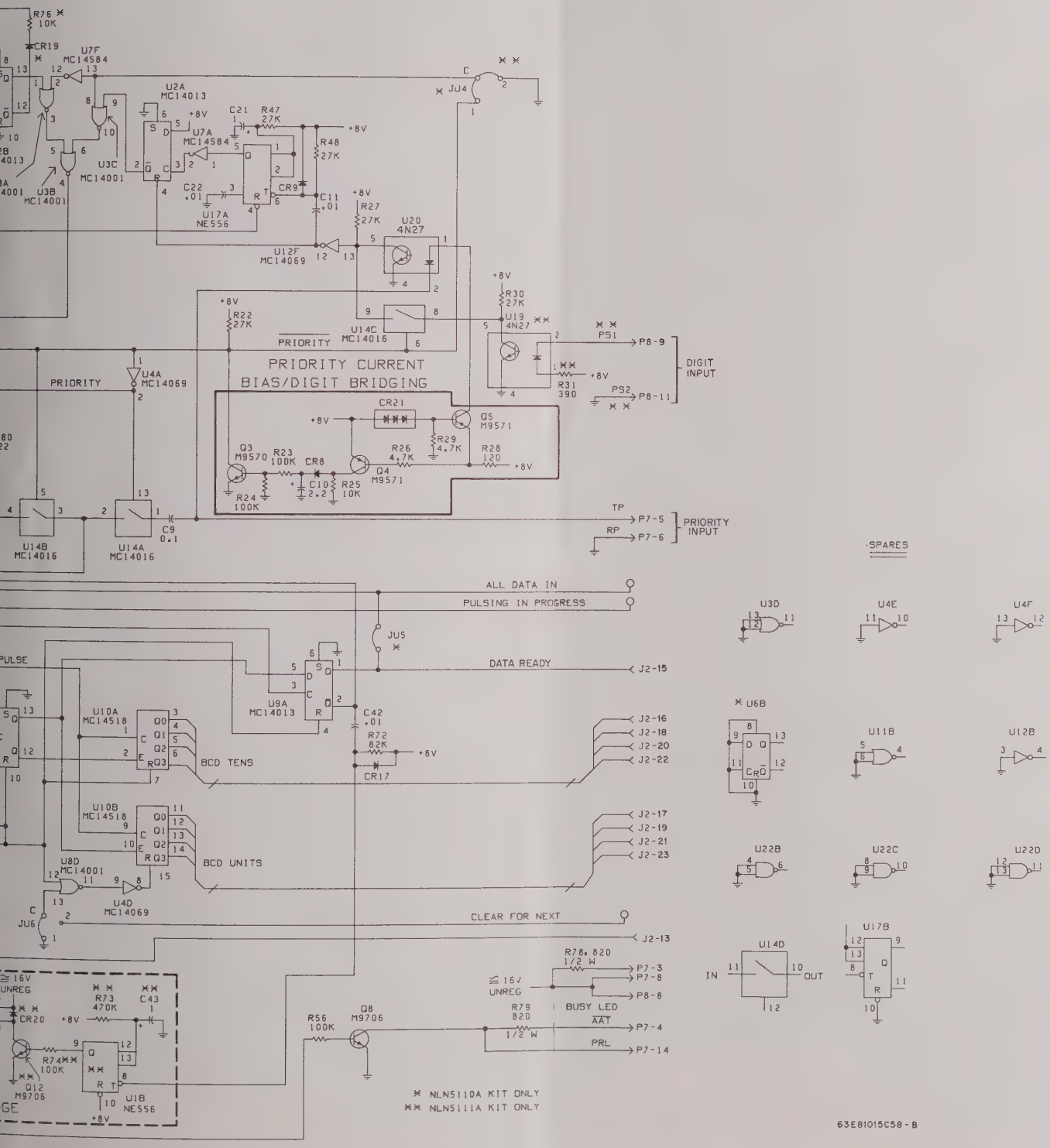
NLN5112A Tone Input Board, Line Level (L)
NLN5113A Tone Input Board, Selector Level (S) PLF-1450-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		CAPACITOR, Fixed: uF ±20%; 20 V unless stated
C1, 2	2383441B19	10
C3	2182428B12	.01 +70-30%; 100 V
C4	2383441B19	10
C5	2100847091	80 pF ±2%; 300 V
C6	2100863299	7000 pF ±1%; 500 V
C7	2100863298	5000 pF ±1%; 500 V
C8	2184008H23	0.22 pF ±10%; 50 V
C9	2184008H08	.02 ±10%; 50 V
C10	2182428B12	.01 +70-30%; 100 V
C11	2184008H08	.02 ±10%; 50 V
C12, 13	2182428B12	.01 +70-30%; 100 V
C14 thru 17	2100864736	1300 pF ±5%; 500 V
C18	0882905G10	.015 uF ±10%; 50 V
C19	2182428B12	.01 +70-30%; 100 V
C20	2383441B19	10
C21	2182428B12	.01 +70-30%; 100 V
C22	2384762H03	10 ±10%; 20 V
C23 thru 31	2383441B19	10
C32	2382783B14	1 ±10%; 15 V
C33	0882906J18	0.1 ±10%; 50 V
C34	2382783B14	1 ±10%; 15 V
C35 thru 42	2383441B19	10
C43	2384762H05	4.7; 25 V
C44	2383441B19	10
C45	2182428B12	.01 +70-30%; 100 V
C46	2383441B19	10
C47	2182428B12	.01 +70-30%; 100 V
C48	2383441B19	10
C49, 50	2182428B12	.01 +70-30%; 100 V
C51	2383441B19	10
C52	2182428B12	.01 +70-30%; 100 V
C53	2383441B19	10
C54	2182428B12	.01 +70-30%; 100 V
C55	2383441B19	10
C56	2182428B12	.01 +70-30%; 100 V
C57	2184008H08	.02 ±10%; 50 V
C58	2182428B12	.01 +70-30%; 100 V
C59, 60	2383441B19	10
		DIODE: See Note
CR1 thru 4	4883329G04	Silicon
CR5 thru 23	4883654H01	Silicon
CR24	4883329G04	Silicon
CR25 thru 29	4883654H01	Silicon
CR30	4883329G04	Silicon
CR31	4883654H01	Silicon
		JACK:
J2	0905259D20	Connector, female; 23 pins
		RELAY:
K1, 2	8005103G01	12 V (NLN5113A only)
		PLUGS:
P7, 8	0905261D01	Molex Connector, male; 15 pins
		TRANSISTOR: See Note
Q1, 2	4800869570	NPN; type M9570
Q3	4800869571	PNP; type M9571
Q4, 5, 6	4800869706	NPN; type M9706
Q7	4800869571	PNP; type M9571
Q8	4800869572	NPN; type M9572
Q9 thru 16	4800869570	NPN; type M9570
Q17	4800869571	PNP; type M9571
Q18	4800869788	PNP; type M9788
Q19	4800869570	NPN; type M9570
		RESISTOR, Fixed: ∩ ±5%; 1/4 W unless stated
R1, 2	0600124A97	100 k
R3	0600124A57	2.2 k
R4	0600124A25	100
R5	0600124A57	2.2 k
R6	0600124A49	1 k
R7 thru 10	0682672B54	249 k ±1%
R11	0600124A59	2.7 k
R12	0600124A49	1 k
R13	0600124A83	27 k
R14	0600124A97	100 k
R15	0600124B22	1 M
R16	0600124A57	2.2 k
R17	0600124A25	100
R18	0600124A57	2.2 k
R19	0600124A49	1 k
R20	0682672B55	825 k ±1%
R21	0683175C04	10.5 k ±1%
R22	0683175C18	15.4 k ±1%
R23	0600124A67	5.6 k
R24	0600124A09	22 (NLN5113A only)
R25	0600124A49	1 k
R26	0600124A83	27 k
R27, 28	0600124A73	10 k
R29	0600124A09	22 (NLN5113A only)
R30	0600124A65	4.7 k
R31	0600124A21	68
R32	0600124A73	10 k
R33	0600125A47	820; 1/2 W
R34 thru 40	0600124A45	680
R41	0600124A01	10
R42	0600124A97	100 k
R43, 44	0600124A65	4.7 k
R45 thru 48	0600124A97	100 k
R49	0600124A57	2.2 k
R50	0600125A47	820; 1/2 W
R51 thru 57	0600124A01	10
R58	0600124A97	100 k
R59	0600124A85	33 k
R60	0600124A89	47 k
R61	0600124A81	22 k
R62	0600124A83	27 k
R63	0600124A69	6.8 k
R64	0600124A51	1.2 k
R65 thru 71	0600124A35	270
R73	0600124A73	10 k
R74	0600124A77	15 k
R75	0600124A61	3.3 k
R76	0600124A67	5.6 k
R77	0683175C20	16.2 k ±1%
R78	0600124A49	1 k
R79	0600124A69	6.8 k
R80	0600124A81	22 k
R81	0600124A69	6.8 k
R82	0600124B24	1.2
R83	0600124B10	330 k
R84	0600124A97	100 k
R85	0600124A83	27 k
R86	0600124B12	390 k
R87	0600124A83	27 k
R88, 89	0600124A97	100 k
		TRANSFORMER:
T1	2584903H01	Audio (NLN5113A only)
		INTEGRATED CIRCUIT:
U1, 2	5184621K21	type MC3403P
U3	5182822F12	CMOS; type M14016
U4	5182822F03	CMOS; type MC14001
U5	5182822F81	CMOS; type MC14419P
U6	5184320A85	type NE556A
U7	5182822F10	CMOS; type MC14013
U8	5182822F40	CMOS; type MC14049
U9	5184320A85	type NE556A
U10	5182822F03	CMOS; type MC14001
U11	5182822F10	CMOS; type MC14013
U12, 13	5184887K30	type MC14175
U14	5182822F03	CMOS; type MC14001
U15	5182822F08	type MC14011
U16	5182822F03	CMOS; type MC14001
U17	5184621K73	type MC78L08CP
U18	5184333G84	Active Filter
U19	5184333G85	Active Filter
U20	5184333G86	Active Filter
U21	5184333G87	Active Filter
U22	5184333G88	Active Filter
U23	5184333G89	Active Filter
U24	5184333G90	Active Filter
		DIODE: See Note
VR1, 2	4883461E30	Zener, 51.0 V (NLN5113A only)
VR3	4882256C58	Zener, silicon
VR4	4883461E02	Zener, silicon
NONREFERENCED ITEMS		
	2905260D01	TERMINAL PINS
	8405906F01	CIRCUIT BOARD

NOTE: For optimum performance, order replacement diodes, transistors, and integrated circuits by Motorola part number only.

TONE INPUT CIRCUIT BOARD DETAIL


LINE LEVEL DIAL DECODER
CLICK DETECTION
LOW PASS FILTER
HIGH PASS-FILTER
SEIZE CONDITION DETECTION
ALLOTMENT TIMER
DCW ALLOTMENT
INVALID AUDIO
TIP
RING
HOLD DETECT
L.O.
CS
CG
S2/RU2
VALID 8
S1/RU1
AUDIO TO/FROM MAIN
SEIZE
CLK 640K
WAIT
PRIORITY
RST
COS
COSG
SERVICE INDICATION DCK/DCW
DH1
DH2
DATA PULSE
AT
GND
+8V
U21A MC3403
U21B MC3403
U21C MC3403
U21D MC3403
U7B MC14584
U7C MC14584
U7D MC14584
U7E MC14584
U13A NE556
U13B NE556
U16D MC14001
U5A NE556
U11A MC14001
U11C MC14001
U11D MC14001
U12E MC14069
U4B MC 14069
U8A MC14001
U8B MC14001
U5B NE556
U16A MC14001
U16B MC14001
U12A MC14069
U15A MC14001
U15C MC14001
U15D MC14001
U16C MC14001
U15B MC140014
U4C MC14069
U8C MC14001
U6A MC14013
U18B NE556
U18A NE556
U1A NE556
U12D MC14069
U22A MC14001
Q1 M9706
Q2 M9570
Q6 M9571
Q7 M9788
Q9 M9572
Q10 M9706
Q11 M9788
Q13 M9706
K1
K2
K4
JU1
JU2
JU3
JU7
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR11
CR12
CR13
CR14
CR16
CR18
VR1
VR2
VR3
T1
ORG
BRN
RED
GRN
YEL
BLU
R1 22
R2 100K
R3 1K
R4 47K
R5 22K
R6 82K
R7 100K
R8 100K
R9 180K
R10 100K
R11 56K
R12 33K
R13 33K
R14 6.8K
R15 12K
R16 4.7K
R17 4.7K
R18 4.7K
R19 10K
R20 10K
R21 15K
R32 6.8K
R33 1.2K
R34 27K
R35 330K
R36 8.2K
R37 100K
R38 56K
R39 100K
R40 10K
R41 100K
R42 100K
R43 100K
R44 100K
R45 27K
R46 1 MEG
R49 100K
R50 100K
R51 27K
R52 1.2 MEG
R53 27K
R54 22K
R55 82K
R57 27K
R58 2.2K
R59 100K
R60 100K
R62 22K
R63 100K
R64 22
R65 18K
R66 27K
R68 82K
R69 470K
R70 100K
R75 22
R77 390K
C1 10
C2 .01
C3 10
C4 10
C5 0.22
C6 .033
C7 22
C8 22
C10 10
C11 0.1
C12 10
C13 10
C14 .01
C15 0.22
C16 0.22
C17 0.1
C18 22
C19 0.22
C20 10
C22 10
C23 0.1
C24 10
C25 .01
C26 .01
C27 .01
C28 10
C29 .01
C30 .01
C31 1
C32 .01
C33 1
C34 .01
C35 10
C36 .01
C37 10
C38 .01
C39 .01
C40 .01
C41 1
C44 22
C45 1
C47 4.7
C48 .01
C48 .01
16V UNREG
AT1
AT2



INTEGRATED CIRCUIT VOLTAGE
& GROUND PIN DESIGNATIONS

REF. DES.	TYPE NUMBER	+V	GND
U1, 5, 13, 17, 18	NE556	14	7
U2, 6, 9	MC14013	14	7
U3, 8, 11, 15, 16	MC14001	14	7
U4, 12	MC14069	14	7
U7	MC14584	14	7
U10	MC14518	16	8
U14	MC14016	14	7
U19, 20	4N27	5	4
U21	MC3403	4	11
U22	MC14011	14	7

EPF-8775-O

NOTES: UNLESS OTHERWISE STATED:
RESISTOR VALUES ARE IN OHMS, k = 1000;
CAPACITOR VALUES ARE IN MICROFARADS (uF);
INDUCTOR VALUES ARE IN HENRYS (H).

EPF-7506-O

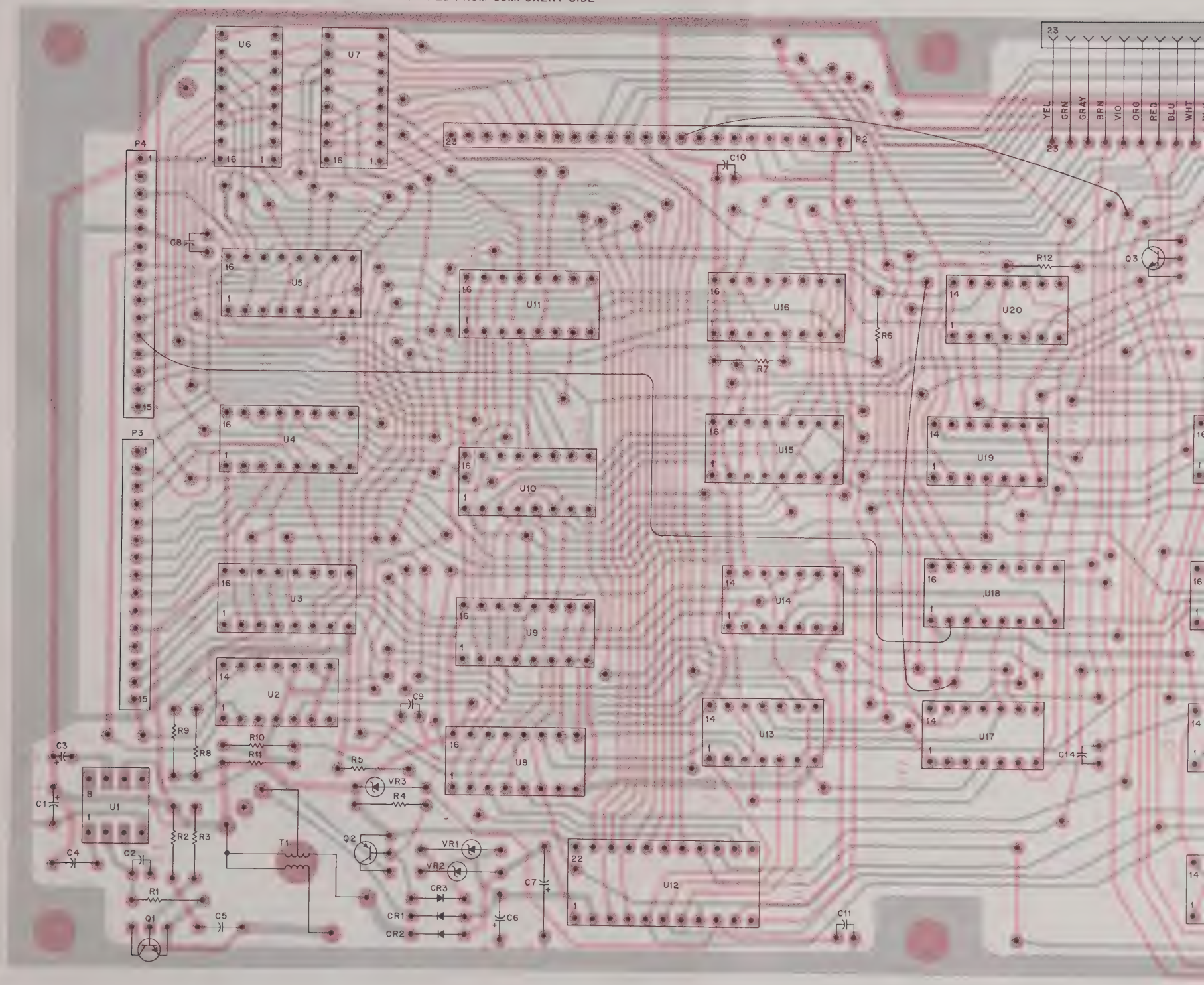
CONNECTOR INFORMATION

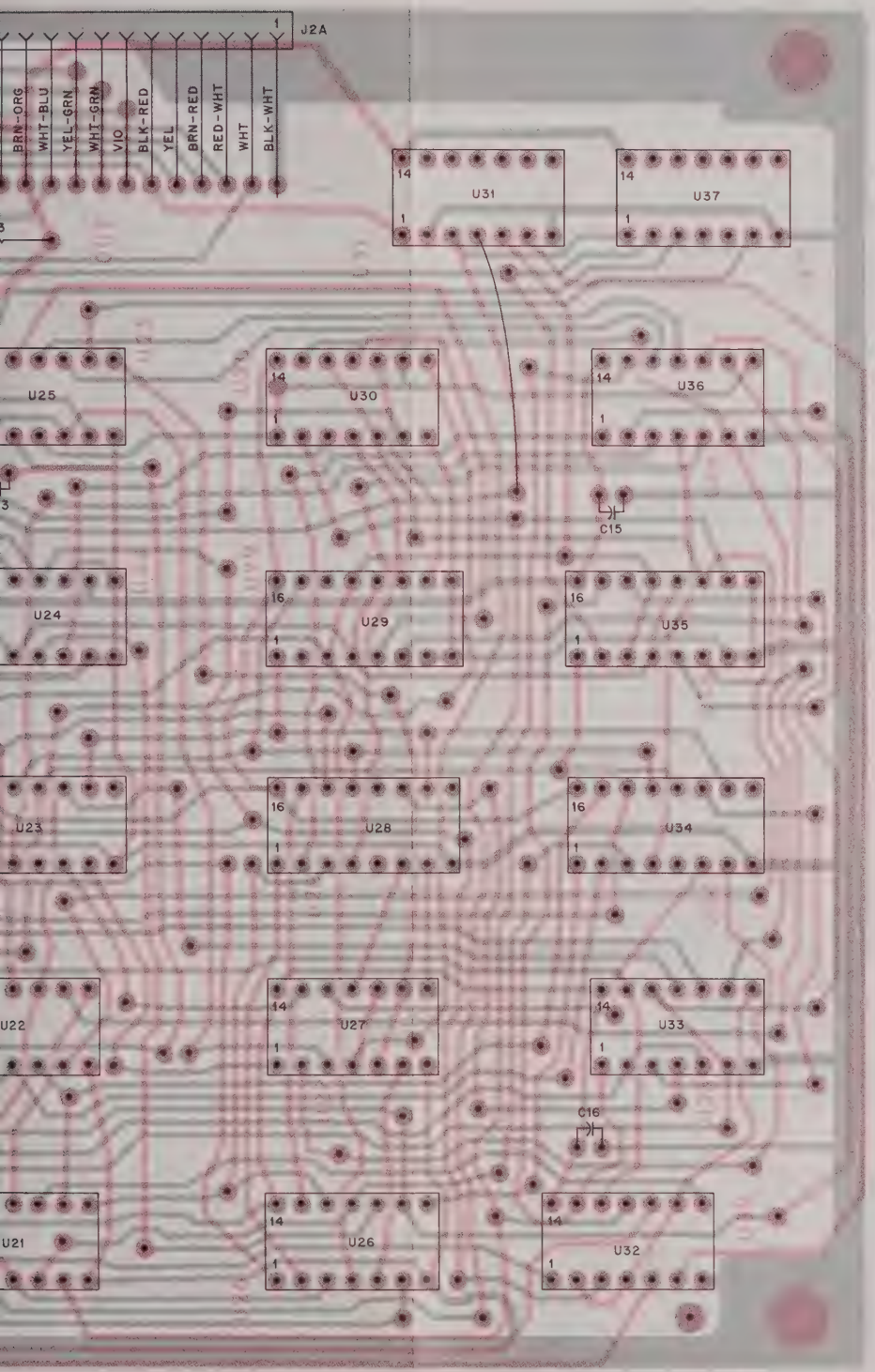
NUMBER	CONNECTS TO / FROM
J / P 1	CHASSIS / MAIN TERMINAL BOARD
J2 / P2 P2A	INPUT BOARD / UNI MAIN MAIN TERMINAL BOARD
J / P 3, 4	MAIN UNI BOARD / UNI DISPLAY BOARD
J / P 5	KEYBOARD / UNI DISPLAY BOARD
J / P 6	CHASSIS / ASI
J / P 7	CHASSIS / INPUT BOARD
P8 / J8 J8A	INPUT BOARD / CHASSIS CABLE TO J9
J9 / P9	CABLE / L.L. INTERFACE BOARD

EPF-9294-O

DIAL PULSE INPUT BOARD SCHEMATIC DIAGRAM

VIEWED FROM COMPONENT SIDE



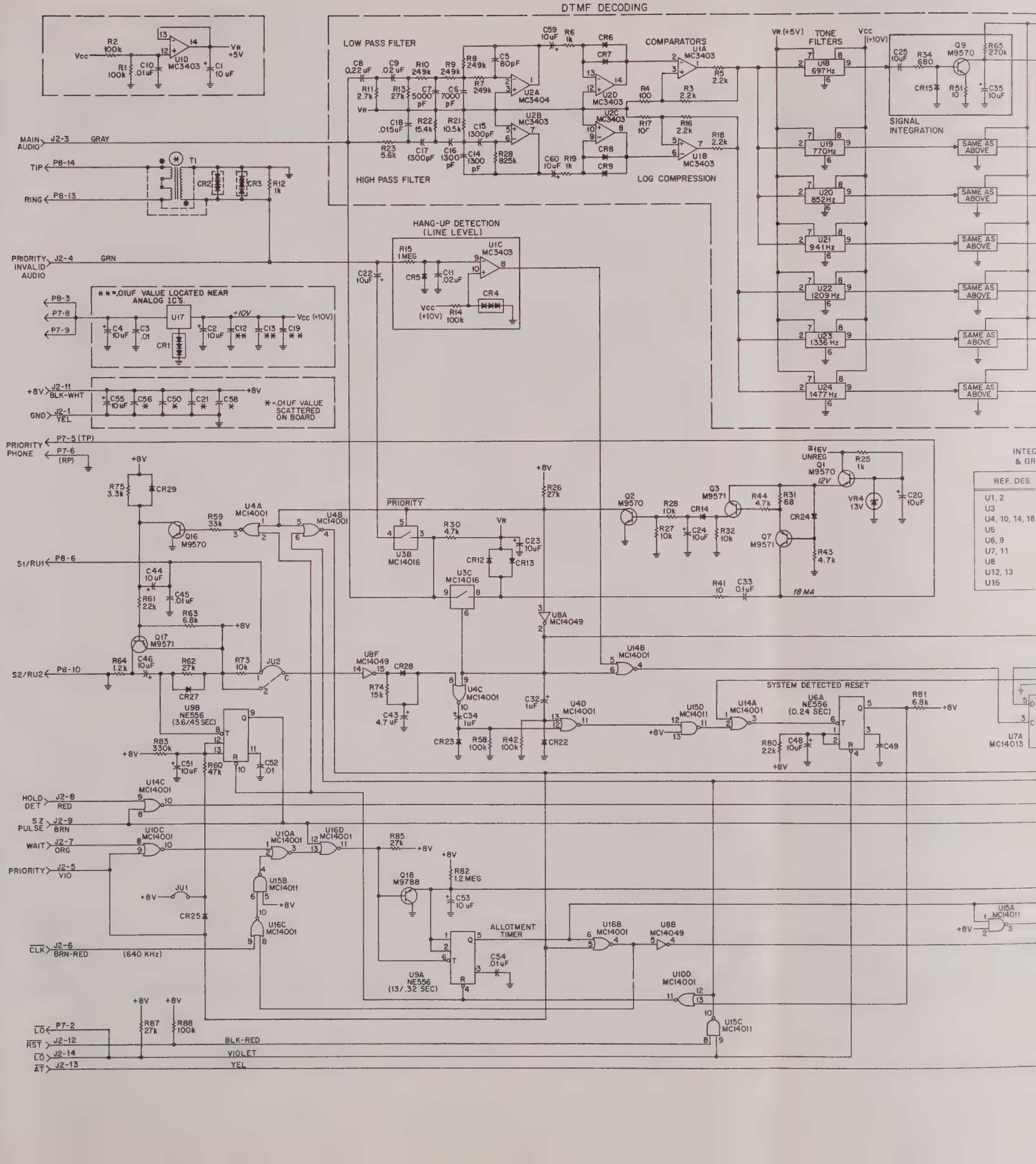


SS EEPF-8785-O
CS EEPF-8786-O
OL EEPF-8787-A

UNIVERSAL NUMBER INTERCHANGE
PRIMARY CIRCUIT BOARD DETAIL

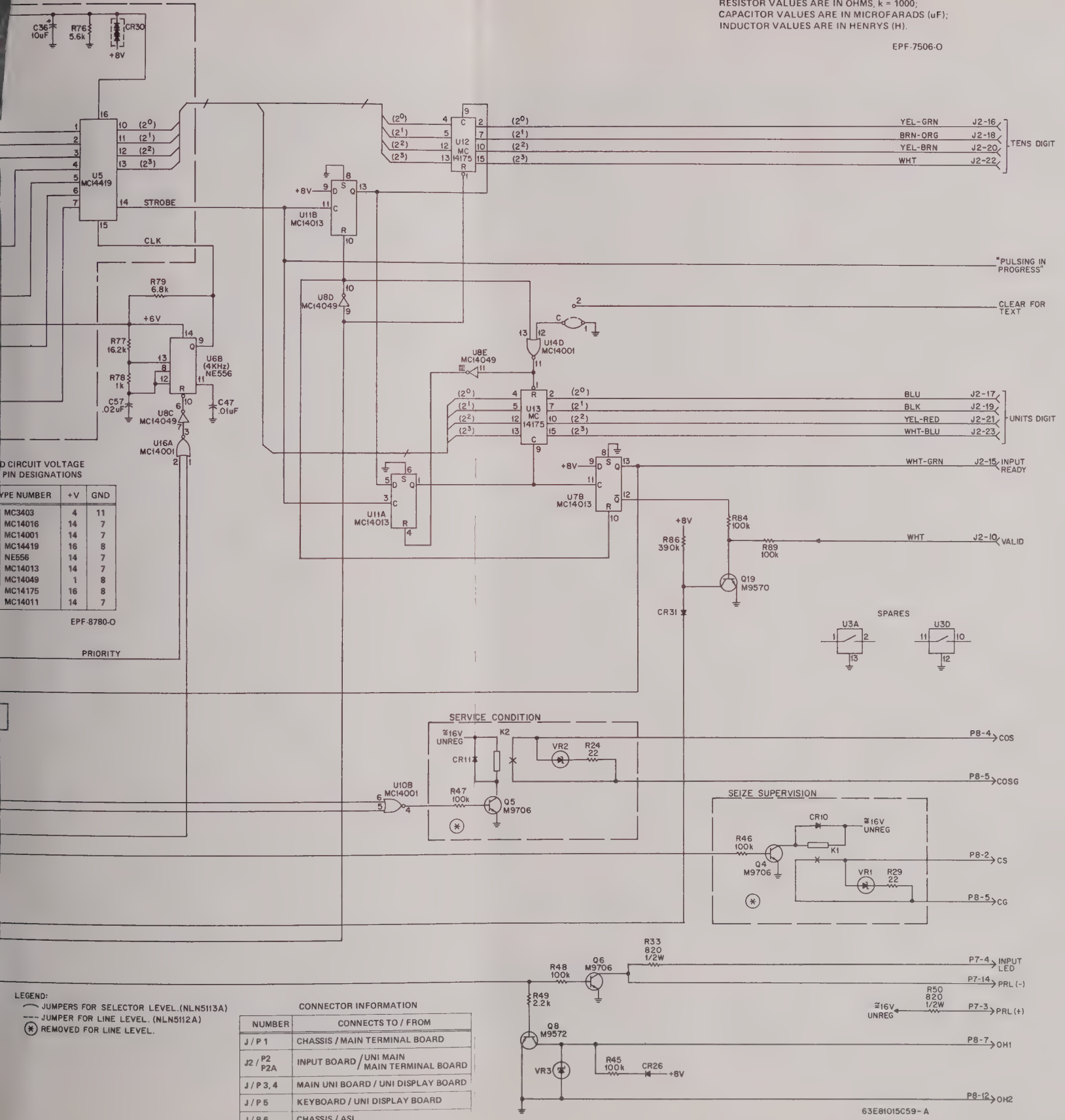
REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		CAPACITOR, Fixed: uF ±10% 50 V unless stated
C1	2383441B28	22 ±20%; 15 V
C2	2184008H01	.01
C3	2383441B28	22 ±20%; 15 V
C4	2182428B04	.01; 100 V
C5	2182428B36	.002; 200 V
C6	2383441B32	47 ±20%; 20 V
C7	2384762H01	4.7; 35 V
C8 thru 11	2184008H01	.01
C13 thru 16	2184008H01	.01
		DIODE: See Note
CR1,2,3	4882420C18	Silicon
		JACK:
J2A	0905259D20	Connector, Female; 23-pin
		PLUG:
P2	0905818F03	Connector, Male; 23-pin
P3,4	0905818F01	Connector, Male; 15-pin
		TRANSISTOR: See Note
Q1	4800869679	NPN; type M9679
Q2	4800869571	PNP; type M9571
Q3	4800869706	NPN; type M9706
		RESISTOR, Fixed: Ω ±5%; 1/4 W
R1	0600124A59	2.7 k
R2	0600124A35	270
R3	0600124A17	47
R4	0600124A59	2.7 k
R5	0600124A37	330
R6 thru 9	0600124A73	10 k
R10	0600124A81	22 k
R11	0600124A85	33 k
R12,13	0600124A97	100 k
		TRANSFORMER:
T1	2405826F01	Pulse; Inductor, pot core
		INTEGRATED CIRCUIT: See Note
U1	5184621K64	type MC3380P
U2	5184320A51	type MC3302P
U3	5184887K71	CMOS; type MC14503BCP
U4	5184887K30	CMOS; type MC14175BCP
U5,6,7	5184887K40	CMOS; type MC14519BCP
U8,9	5184887K67	CMOS; type MC14052BCP
U10	5184887K40	CMOS; type MC14519BCP
U11	5184887K30	CMOS; type MC14175BCP
U12	5184865G15	type ER3401
U13	5182822F44	CMOS; type MC14081CP
U14	5184887K13	CMOS; type MC14013BCP
U15,16	5184887K30	CMOS; type MC14175BCP
U17	5184887K28	CMOS; type MC14073BCP
U18	5184887K01	CMOS; type MC14049BCP
U19	5184887K13	CMOS; type MC14013BCP
U20,21	5182822F43	CMOS; type MC14071CP
U22	5184887K29	CMOS; type MC14075BCP
U23	5184887K20	CMOS; type MC14028BCP
U24	5184887K21	CMOS; type MC14027BCP
U25	5182822F44	CMOS; type MC14081CP
U26,27	5184887K29	CMOS; type MC14075BCP
U28	5184887K20	CMOS; type MC14028BCP
U29	5184887K21	CMOS; type MC14027BCP
U30	5182822F43	CMOS; type MC14071CP
U31	5182822F29	CMOS; type MC14024CP
U32	5182822F44	CMOS; type MC14081CP
U33	5184887K08	CMOS; type MC14011BCP
U34	5184887K20	CMOS; type MC14028BCP
U35	5184887K21	CMOS; type MC14027BCP
U36	5184887K29	CMOS; type MC14075BCP
U37	5182822F29	CMOS; type MC14024CP
		DIODE: See Note
VR1	4883461E01	16 V Zener
VR2	4883461E33	18 V Zener
VR3	4882256C51	5.1 V Zener
	NONREFERENCED ITEMS	
	0210239A03	NUT, Hex; 4-40
	0310129A22	SCREW, Slotted; 4-40 x 7/8"
	2905260D01	TERMINAL, Single contact
	8405810F01	CIRCUIT BOARD

NOTE: For optimum performance, order replacement diodes, transistors, and integrated circuits by Motorola part number only.


DTMF DECODING
LOW PASS FILTER
HIGH PASS FILTER
COMPARATORS
LOG COMPRESSION
TONE FILTERS
SIGNAL INTEGRATION
HANG-UP DETECTION (LINE LEVEL)
SYSTEM DETECTED RESET
ALLOTMENT TIMER
MAIN AUDIO J2-3 GRAY
TIP P8-14
RING P8-13
PRIORITY INVALID AUDIO J2-4 GRN
PRIORITY PHONE P7-5 (TP)
P7-6 (RP)
S1/RU1 P8-6
S2/RU2 P8-10
HOLD DET J2-8 RED
SZ PULSE J2-9 BRN
WAIT J2-7 ORG
PRIORITY J2-5 VIO
CLK J2-6 BRN-RED (640 KHz)
LO P7-2
RST J2-12 BLK-RED
LO J2-14 VIOLET
AT J2-13 YEL
+8V J2-11 BLK-WHT
GND J2-1 YEL
*=.01UF VALUE SCATTERED ON BOARD
**=.01UF VALUE LOCATED NEAR ANALOG IC'S.
U1D MC3403
U2A MC3404
U2B MC3403
U2C MC3403
U2D MC3403
U1A MC3403
U1B MC3403
U1C MC3403
U18 697Hz
U19 770Hz
U20 852Hz
U21 941Hz
U22 1209Hz
U23 1336Hz
U24 1477Hz
SAME AS ABOVE
U4A MC14001
U4B MC14001
U4C MC14001
U4D MC14001
U14A MC14001
U14B MC14001
U14C MC14001
U10A MC14001
U10B MC14001
U10C MC14001
U10D MC14001
U16D MC14001
U38 MC14016
U3C MC14016
U8A MC14049
U8B MC14049
U8F MC14049
U15A MC14011
U15B MC14011
U15C MC14011
U15D MC14011
U9A NE556 (13/.32 SEC)
U9B NE556 (3.6/45 SEC)
U6A NE556 (0.24 SEC)
U7A MC14013
U17
Q1 M9570 12V
Q2 M9570
Q3 M9571
Q7 M9571
Q9 M9570
Q16 M9570
Q17 M9571
Q18 M9788
18 MA
VR4 13V
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR12
CR13
CR14
CR15
CR22
CR23
CR24
CR25
CR27
CR28
CR29
T1
JU1
JU2
REF. DES.
U1, 2
U3
U4, 10, 14, 16
U5
U6, 9
U7, 11
U8
U12, 13
U15

RESISTOR VALUES ARE IN OHMS, k = 1000;
CAPACITOR VALUES ARE IN MICROFARADS (uF);
INDUCTOR VALUES ARE IN HENRYS (H).

EPF-7506-O



D CIRCUIT VOLTAGE
PIN DESIGNATIONS

YPE NUMBER	+V	GND
MC3403	4	11
MC14016	14	7
MC14001	14	7
MC14419	16	8
NE556	14	7
MC14013	14	7
MC14049	1	8
MC14175	16	8
MC14011	14	7

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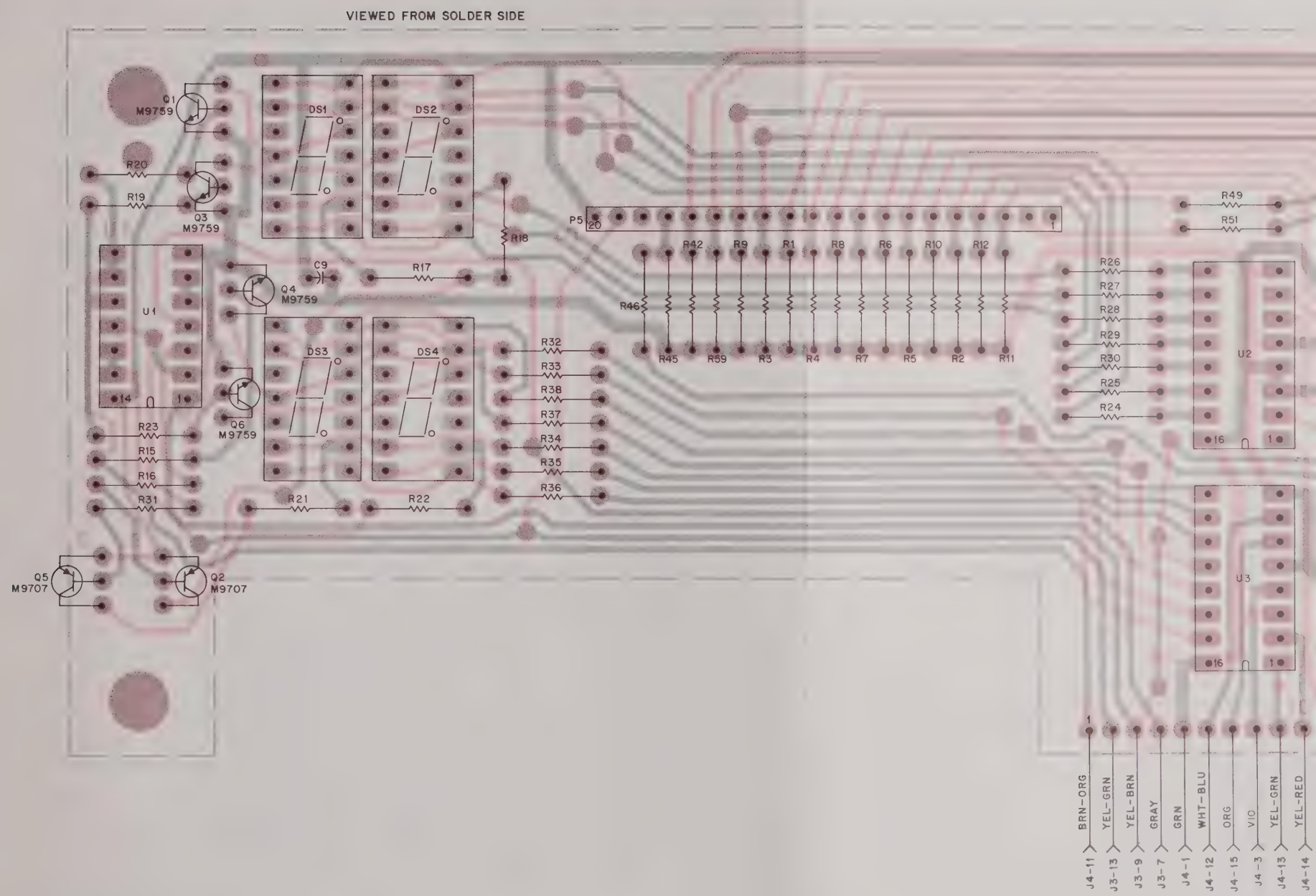
LEGEND:
- ⌒ JUMPERS FOR SELECTOR LEVEL.(NLN5113A)
- ⌒ JUMPER FOR LINE LEVEL. (NLN5112A)
- (*) REMOVED FOR LINE LEVEL.

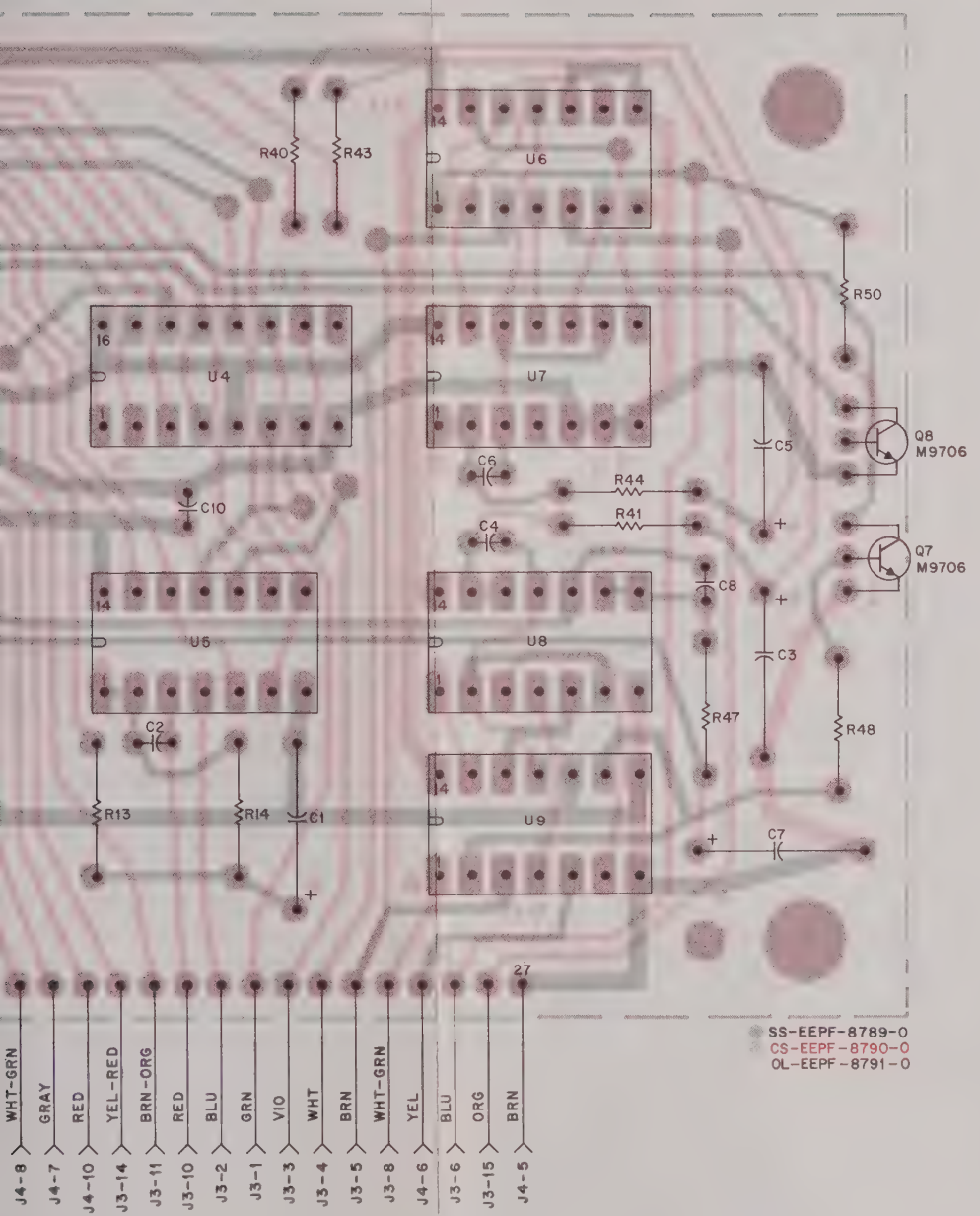
CONNECTOR INFORMATION

NUMBER	CONNECTS TO / FROM
J / P 1	CHASSIS / MAIN TERMINAL BOARD
J2 / P2 P2A	INPUT BOARD / UNI MAIN MAIN TERMINAL BOARD
J / P 3, 4	MAIN UNI BOARD / UNI DISPLAY BOARD
J / P 5	KEYBOARD / UNI DISPLAY BOARD
J / P 6	CHASSIS / ASI
J / P 7	CHASSIS / INPUT BOARD
P8 / J8 J8A	INPUT BOARD / CHASSIS CABLE TO J9
J9 / P9	CABLE / L.L. INTERFACE BOARD

EPF-9294-O

TONE INPUT BOARD SCHEMATIC DIAGRAM


VIEWED FROM SOLDER SIDE
Q1 M9759
Q3 M9759
Q4 M9759
Q6 M9759
Q5 M9707
Q2 M9707
DS1
DS2
DS3
DS4
U1
U2
U3
P5
20
1
14
16
R20
R19
R18
C9
R17
R23
R15
R16
R31
R21
R22
R32
R33
R38
R37
R34
R35
R36
R42
R9
R1
R8
R6
R10
R12
R46
R45
R59
R3
R4
R7
R5
R2
R11
R49
R51
R26
R27
R28
R29
R30
R25
R24
BRN-ORG
YEL-GRN
YEL-BRN
GRAY
GRN
WHT-BLU
ORG
VIO
YEL-GRN
YEL-RED
J4-11
J3-13
J3-9
J3-7
J4-1
J4-12
J4-15
J4-3
J4-13
J4-14

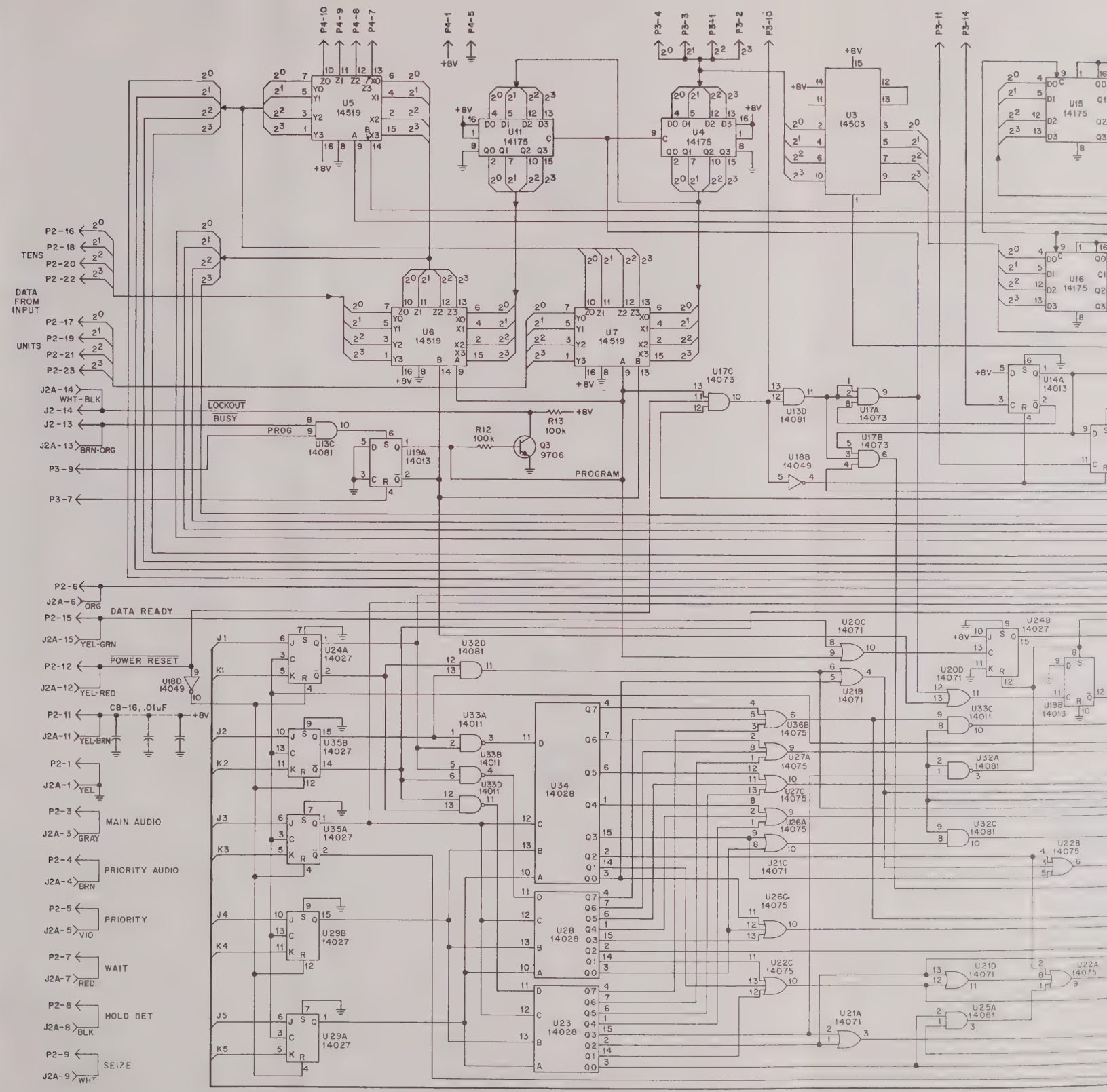


UNIVERSAL NUMBER INTERCHANGE DISPLAY CIRCUIT BOARD DETAIL

NLN5116A Universal Number Interchange Display Assembly PLF-1453-A

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		CAPACITOR, Fixed: uF ±10%, 50 V unless stated
C1	2384762H01	4.7; 35 V
C2	2184008H19	.022 ±20%
C3	2384762H01	4.7; 35 V
C4	2184008H19	.022 ±20%
C5	2384762H01	4.7; 35 V
C6	2184008H19	.022 ±20%
C7	2384762H01	4.7; 35 V
C8	2184008H19	.022 ±20%
C9,10	2184008H01	.01
		DIODE: See Note
CR1,2	4805174A01	Light emitting
DS1 thru 4	4805812E01	7 Segment Array
		JACK:
J3,4	0905259D01	Connector Wafer, 15-pin
J5	0905818F02	Connector Wafer; 20-pin
		PLUG:
P5	0905259D04	Connector Board, 20-pin
		TRANSISTOR: See Note
Q1	4800869759	NPN; type M9759
Q2	4800869707	PNP; type M9707
Q3,4	4800869759	NPN; type M9759
Q5	4800869707	PNP; type M9707
Q6	4800869759	NPN; type M9759
Q7,8	4800869706	NPN; type M9706
		RESISTOR, Fixed: Ω ±5%, 1/4 W unless stated
R1 thru 12	0600124A97	100 k
R13	0600124A73	10 k
R14	0600124B06	220 k
R15	0600124A73	10 k
R16	0600124A97	100 k
R17,18	0600124A41	470
R19,20	0600124A73	10 k
R21,22	0600124A41	470
R23	0600124A73	10 k
R24 thru 30	0600124A35	270
R31	0600124A97	100 k
R32 thru 38	0600124A35	270
R39,40	0600124A73	10 k
R41	0600124B06	220 k
R42,43	0600124A73	10 k
R44	0600124B06	220 k
R45,46	0600124A73	10 k
R47	0600124B06	220 k
R48	0600124A97	100 k
R49	0600124A41	470
R50	0600124A97	100 k
R51	0600124A41	470
		SWITCH:
S1,2,3	4005825F01	Pushbutton
		INTEGRATED CIRCUIT:
U1	5184887K08	CMOS; type MC14011
U2,3	5184887K59	CMOS; type MC14511
U4	5184887K63	CMOS; type MC14532
U5	5182822F43	CMOS; type MC14071
U6	5184887K13	CMOS; type MC14013
U7,8	5182822F44	CMOS; type MC14081
U9	5184887K13	CMOS; type MC14013
NONREFERENCED ITEMS		
	0105824F01	KEYBOARD; 12 position
	0200007041	NUT; Hex, 2-56 x 3/16 x 1/16
	0300007342	SCREW; 6-32 x 5/8
	0300007362	SCREW, machine; 6-32 x 1/2
	0400001719	WASHER, Flat; .141 x .375 x .030
	0400007666	LOCKWASHER
	0400138322	WASHER, Flat; .093 x .165 x .010
	0400400139	LOCKWASHER
	0905388E01	SOCKET, for DS1 thru 4
	2905260D01	TERMINAL
	4282143C02	CLAMP, Cable
	5505475E01	CONNECTOR, Key
	6105815F01	DISPLAY, Window
	6405827F01	PANEL, Front
	8405659F01	CIRCUIT BOARD, Display

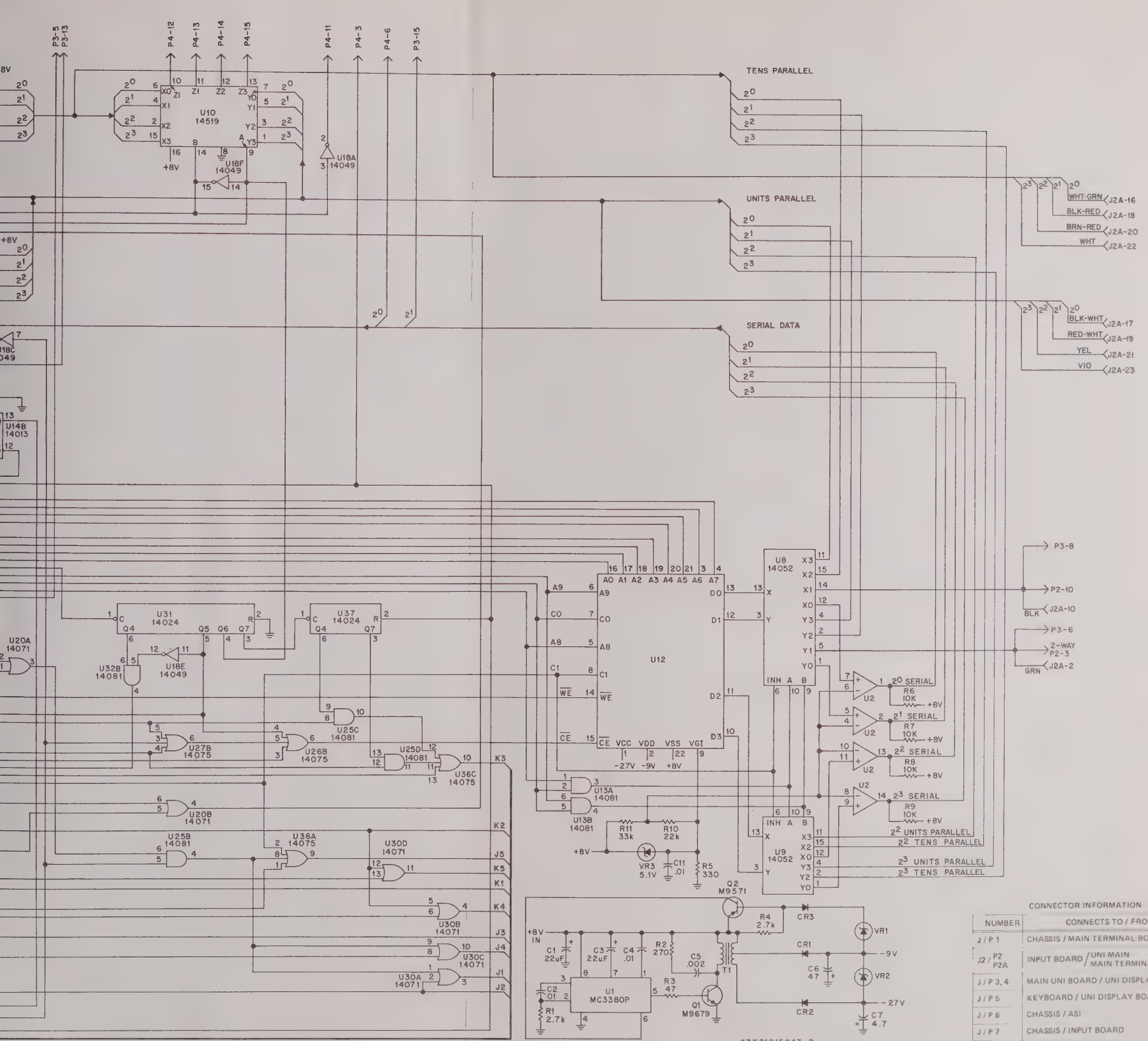
NOTE: For optimum performance, order replacement diodes and transistors by Motorola part number only.



REF DES	TYPE
U1	MC
U2	MC
U3	MC
U4,11,15,16	MC
U5,6,7,10	MC
U8,9	MC
U12	FR
U13,25,32	MC

NOTES: UNLESS OTHERWISE STATED:
RESISTOR VALUES ARE IN OHMS, k = 1000;
CAPACITOR VALUES ARE IN MICROFARADS (uF);
INDUCTOR VALUES ARE IN HENRYS (H).

EPF-7506 O



CONNECTOR INFORMATION

NUMBER	CONNECTS TO / FROM
J / P 1	CHASSIS / MAIN TERMINAL BOARD
J2 / P2 P2A	INPUT BOARD / UNI MAIN MAIN TERMINAL BOARD
J / P 3, 4	MAIN UNI BOARD / UNI DISPLAY BOARD
J / P 5	KEYBOARD / UNI DISPLAY BOARD
J / P 6	CHASSIS / ASI
J / P 7	CHASSIS / INPUT BOARD
P8 / J8 J8A	INPUT BOARD / CHASSIS CABLE TO J9
J9 / P9	CABLE / L.L. INTERFACE BOARD

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INTEGRATED CIRCUIT VOLTAGE & GROUND PIN DESIGNATIONS

UMBER	+ 8 V	GND
380	8	4
302	3	12
4503	16	8
4175	16	8
4519	16	8
4052	16	8
400	*	*
4081	14	7

U14,19	MC14013	14	7
U17	MC14073	14	7
U18	MC14049	1	8
U20,21,30	MC14071	14	7
U22,26,27,36	MC14075	14	7
U23,28,34	MC14028	16	8
U24,29,35	MC14027	16	8
U31,37	MC14024	14	7
U33	MC14011	14	7

*Refer to schematic diagram pin labeling.

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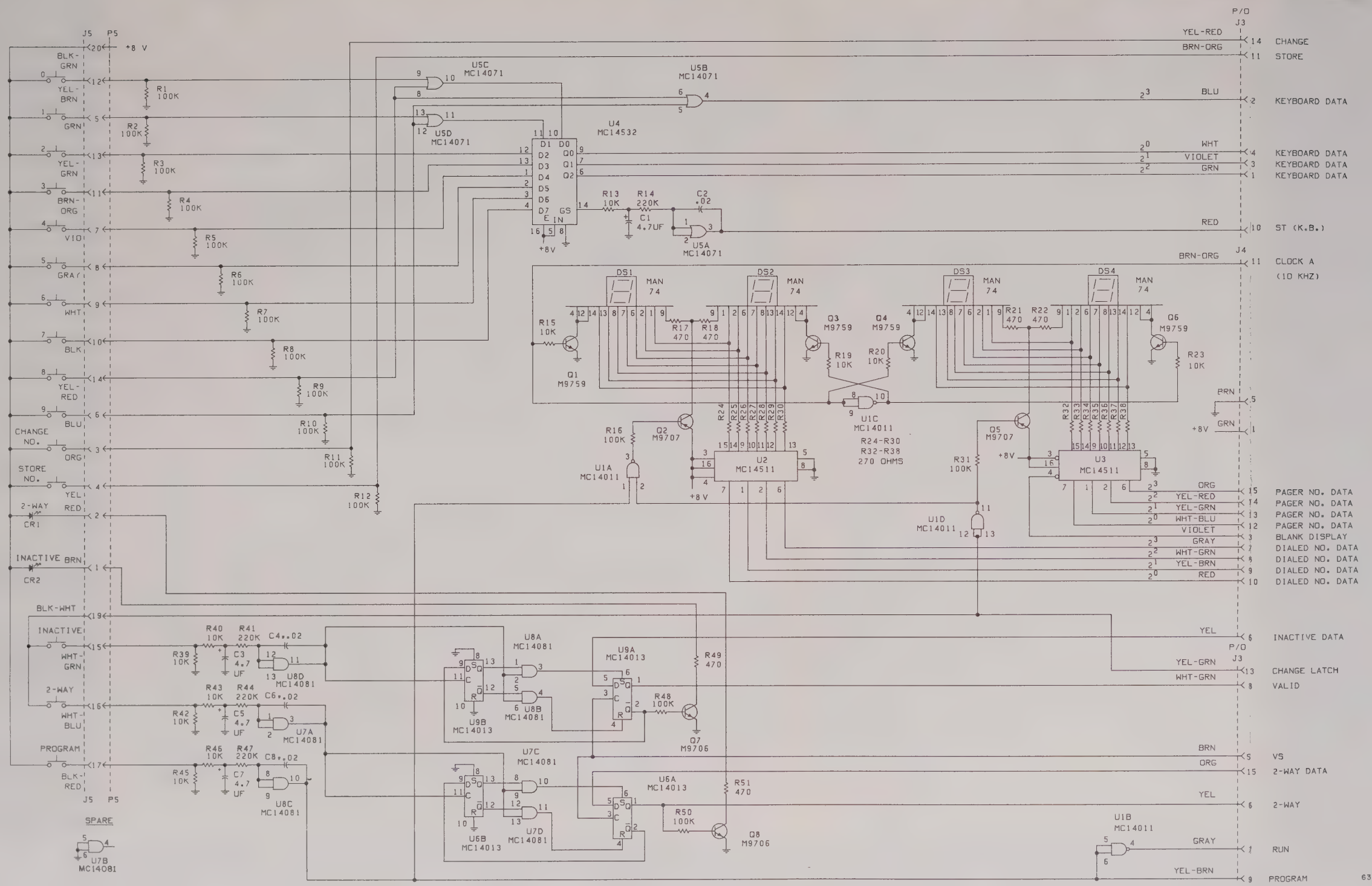

CONNECTOR INFORMATION

NUMBER	CONNECTS TO / FROM
J / P 1	CHASSIS / MAIN TERMINAL BOARD
J2 / P2 P2A	INPUT BOARD / UNI MAIN MAIN TERMINAL BOARD
J / P 3, 4	MAIN UNI BOARD / UNI DISPLAY BOARD
J / P 5	KEYBOARD / UNI DISPLAY BOARD
J / P 6	CHASSIS / ASI
J / P 7	CHASSIS / INPUT BOARD
P8 / J8 J8A	INPUT BOARD / CHASSIS CABLE TO J9
J9 / P9	CABLE / L.L. INTERFACE BOARD

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REF.DES.	TYPE NUMBER	+V	GND
U1	MC14011	14	7
U2,U3	MC14511	16	8
U4	MC14532	16	8
U5	MC14071	14	7
U6,U9	MC14013	14	7
U7,U8	MC14081	14	7

63E81015C44-O

NOTES: UNLESS OTHERWISE STATED:
RESISTOR VALUES ARE IN OHMS, k = 1000;
CAPACITOR VALUES ARE IN MICROFARADS (uF);
INDUCTOR VALUES ARE IN HENRYS (H).

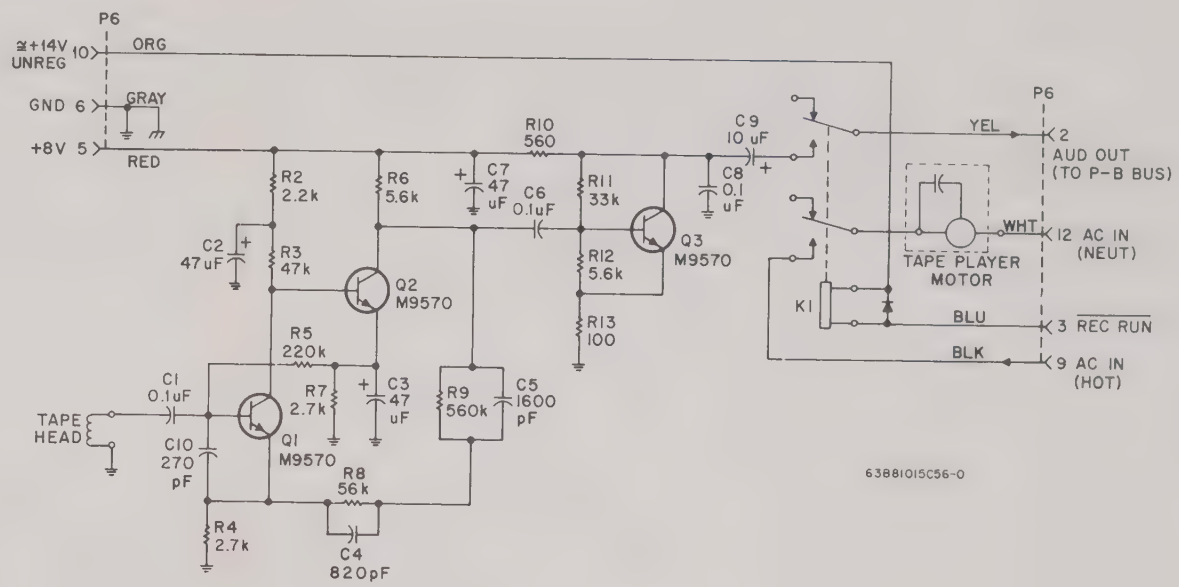
EPF-7506-O

UNIVERSAL NUMBER INTERCHANGE DISPLAY BOARD SCHEMATIC DIAGRAM

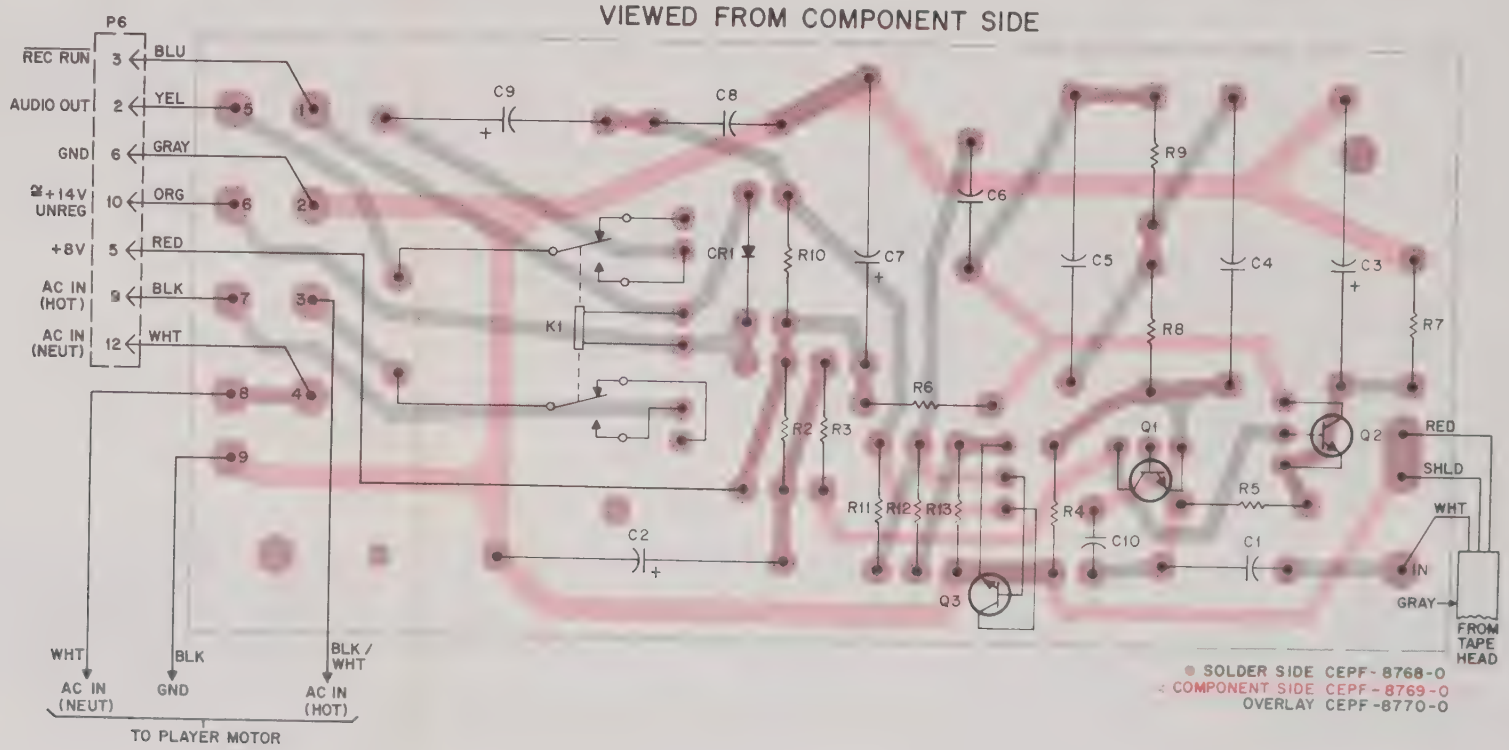
NLN5107A Tape Player and Amplifier Kit PLF-1448-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0105426D01	TAPE DECK
	0105958D02	AMPLIFIER (Includes the following):
		CAPACITOR, Fixed: uF ±50 -10%; 25 V unless stated
C1	0882905G07	0.1 ±10%; 50 V
C2, 3	2382256J01	47
C4	0882163J03	820 pF ±5%; 63 V
C5	0882163J05	1600 pF ±5%; 33 V
C6	0882905G07	0.1 ±10%; 50 V
C7	2382256J01	47
C8	0882905G07	0.1 ±10%; 50 V
C9	2382256J03	10
C10	2184511B28	270 pF ±10%; 50 V
		DIODE: See Note
CR1	4883654H01	Silicon
		RELAY:
K1	8005416D01	2-Pole, Double-Throw; 12 V
		TRANSISTOR: See Note
Q1, 2, 3	4800869570	NPN; type M9570
		RESISTOR, Fixed: Ω ±5%; 1/4 W unless stated
R1		Not Used
R2	0600124A57	2.2 k
R3	0600124A89	47 k
R4	0600124A59	2.7 k
R5	0600124B06	220 k
R6	0600124A67	5.6 k
R7	0600124A59	2.7 k
R8	0600124A91	56 k
R9	0600124B16	560 k
R10	0600124A43	560
R11	0600124A85	33 k
R12	0600124A67	5.6 k
R13	0600124A25	100
		NONREFERENCED ITEMS
		(Part of Amplifier Assembly)
	0200007005	NUT, Hex; 6-32 x 1/4" x 3/32"
	0300007229	SCREW, Slotted; 6-32 x 3/8"
	0400001719	WASHER, Flat; .141 - .375 - .030
	0400009795	LOCKWASHER, #6
	1405622D01	INSULATOR, Recorder
	1482833H01	INSULATOR, Plug
	2982335A02	TERMINAL, Male
	4282143C01	CLAMP, Cable
	8405403D01	CIRCUIT BOARD
		(Part of Tape Player Kit)
	0200007019	NUT, Hex; 4-40 x 1/4" x 3/32"
	0210054A59	NUT, Clip-on; 6-32
	0300001930	SCREW, Slotted; 4-40 x 3/8"
	0300007229	SCREW, Slotted; 6-32 x 3/8"
	0400007607	WASHER, Flat; .125 - .281 - .027
	0400007666	LOCKWASHER, External tooth; #6
	0400007667	LOCKWASHER, External tooth; #4
	0705828F01	BRACKET, Support
	4210217A02	STRAP, Tie

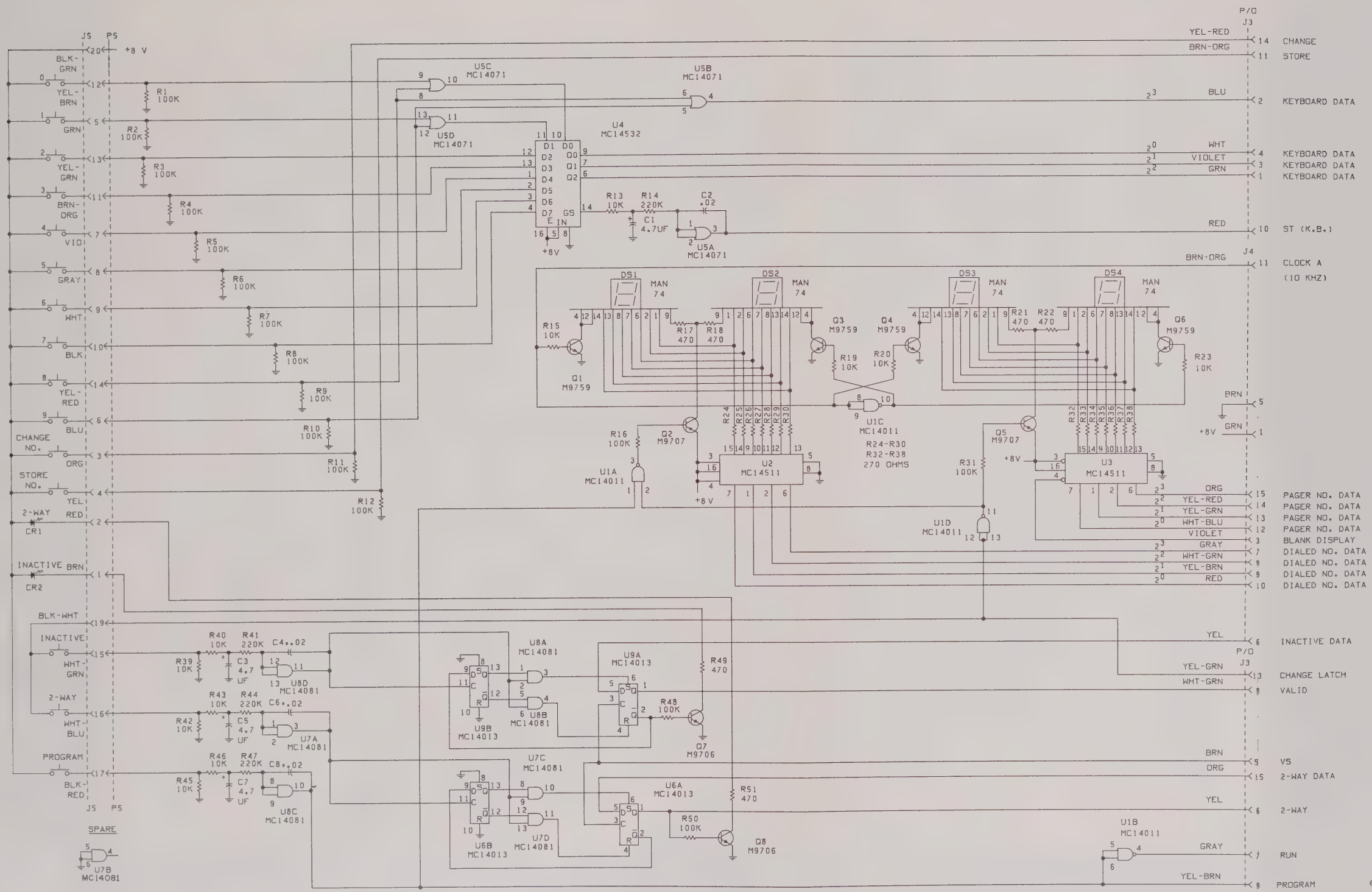
NOTE: For optimum performance, order replacement diodes and transistors by Motorola part number only.



TAPE PLAYER & AMPLIFIER (ASI) SCHEMATIC DIAGRAM



TAPE PLAYER & AMPLIFIER (ASI) CIRCUIT BOARD DETAIL



CONNECTOR INFORMATION

NUMBER	CONNECTS TO / FROM
J / P 1	CHASSIS / MAIN TERMINAL BOARD
J2 / P2 P2A	INPUT BOARD / UNI MAIN MAIN TERMINAL BOARD
J / P 3, 4	MAIN UNI BOARD / UNI DISPLAY BOARD
J / P 5	KEYBOARD / UNI DISPLAY BOARD
J / P 6	CHASSIS / ASI
J / P 7	CHASSIS / INPUT BOARD
P8 / J8 J8A	INPUT BOARD / CHASSIS CABLE TO J9
J9 / P9	CABLE / L.L. INTERFACE BOARD

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REF.DES.	TYPE NUMBER	+V	GND
U1	MC14011	14	7
U2,U3	MC14511	16	8
U4	MC14532	16	8
U5	MC14071	14	7
U6,U9	MC14013	14	7
U7,U8	MC14081	14	7

NOTES: UNLESS OTHERWISE STATED:
RESISTOR VALUES ARE IN OHMS, k = 1000;
CAPACITOR VALUES ARE IN MICROFARADS (uF);
INDUCTOR VALUES ARE IN HENRYS (H).

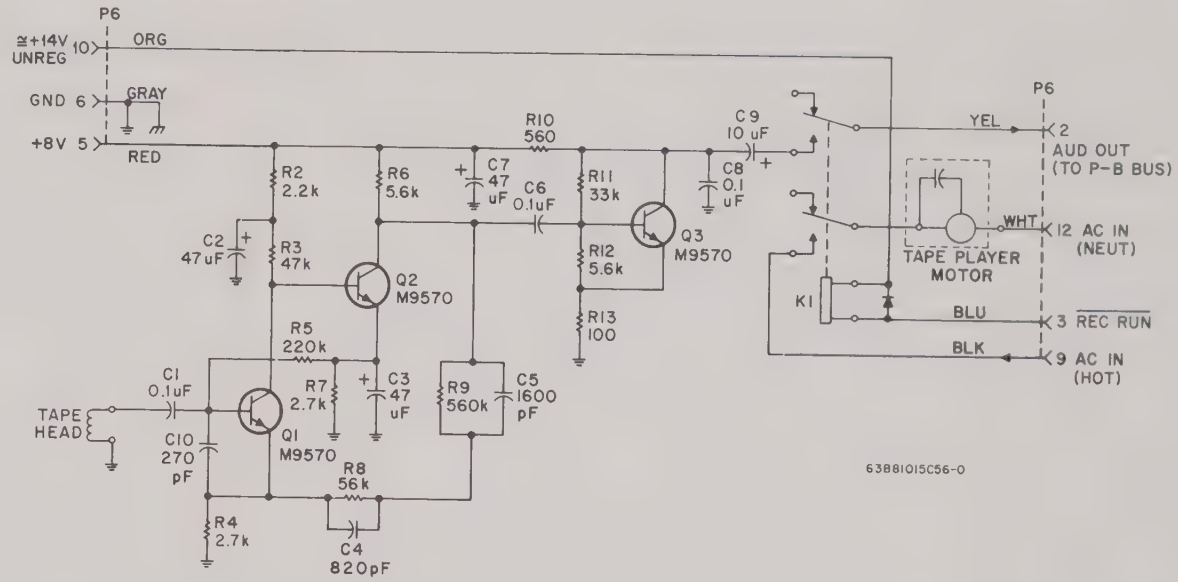
EPF-7506-O

UNIVERSAL NUMBER INTERCHANGE DISPLAY BOARD SCHEMATIC DIAGRAM

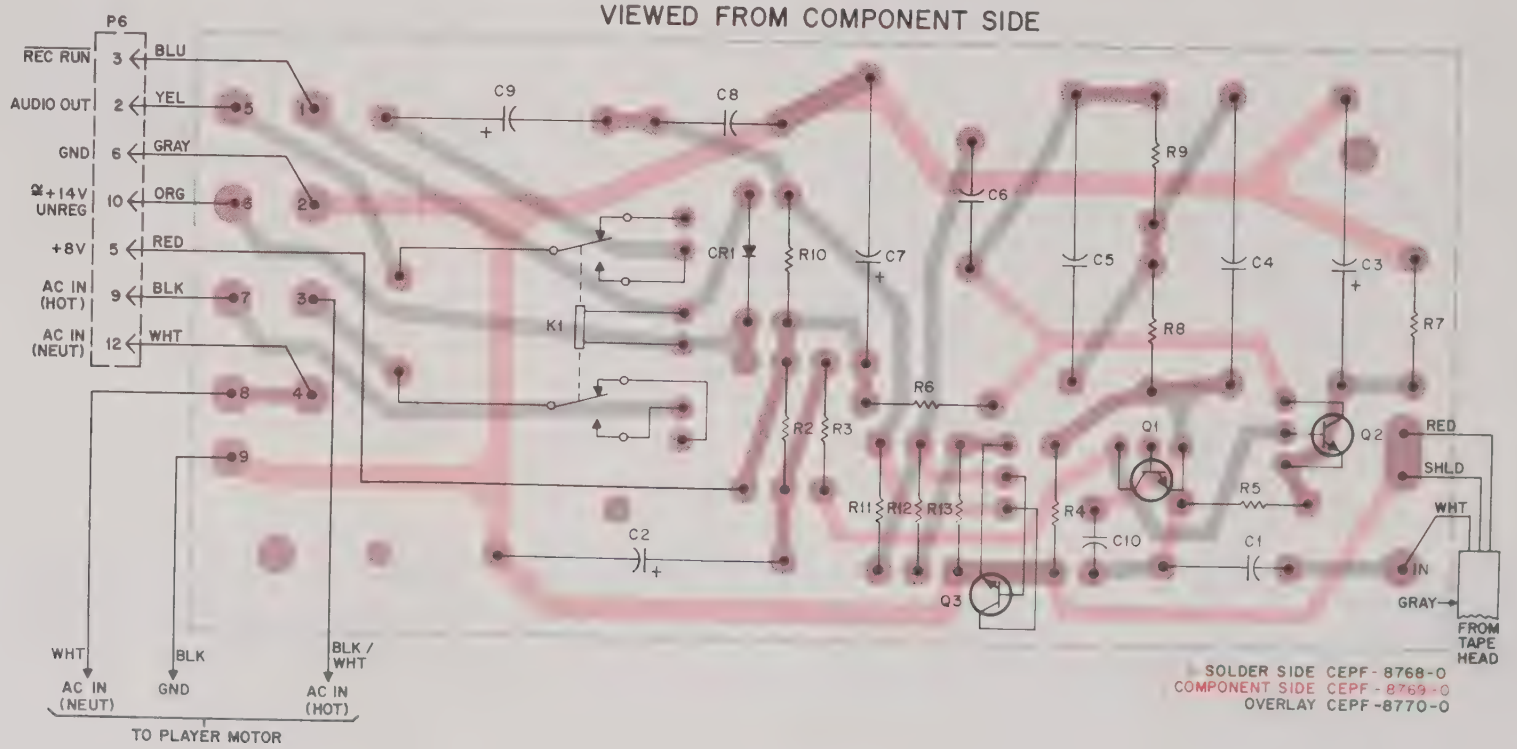
NLN5107A Tape Player and Amplifier Kit PLF-1448-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	0105426D01	TAPE DECK
	0105958D02	AMPLIFIER (Includes the following):
		CAPACITOR, Fixed: uF +50 -10%; 25 V unless stated
C1	0882905G07	0.1 ±10%; 50 V
C2, 9	2382256J01	47
C4	0882163J03	820 pF ±5%; 63 V
C5	0882163J05	1600 pF ±5%; 33 V
C6	0882905G07	0.1 ±10%; 50 V
C7	2382256J01	47
C8	0882905G07	0.1 ±10%; 50 V
C9	2382256J03	10
C10	2184511B28	270 pF ±10%; 50 V
		DIODE: See Note
CR1	4883654H01	Silicon
		RELAY:
K1	8005416D01	2-Pole, Double-Throw; 12 V
		TRANSISTOR: See Note
Q1, 2, 3	4800869570	NPN; type M9570
		RESISTOR, Fixed: Ω ±5%; 1/4 W unless stated
R1		Not Used
R2	0600124A57	2.2 k
R3	0600124A89	47 k
R4	0600124A59	2.7 k
R5	0600124B06	220 k
R6	0600124A67	5.6 k
R7	0600124A59	2.7 k
R8	0600124A91	56 k
R9	0600124B16	560 k
R10	0600124A43	560
R11	0600124A85	33 k
R12	0600124A67	5.6 k
R13	0600124A25	100
	NONREFERENCED ITEMS	
	(Part of Amplifier Assembly)	
	0200007005	NUT, Hex; 6-32 x 1/4" x 3/32"
	0300007229	SCREW, Slotted; 6-32 x 3/8"
	0400001719	WASHER, Flat; .141 - .375 - .030
	0400009795	LOCKWASHER, #6
	1405622D01	INSULATOR, Recorder
	1482833H01	INSULATOR, Plug
	2982335A02	TERMINAL, Male
	4282143C01	CLAMP, Cable
	8405403D01	CIRCUIT BOARD
	(Part of Tape Player Kit)	
	0200007019	NUT, Hex; 4-40 x 1/4" x 3/32"
	0210054A59	NUT, Clip-on; 6-32
	0300001930	SCREW, Slotted; 4-40 x 3/8"
	0300007229	SCREW, Slotted; 6-32 x 3/8"
	0400007607	WASHER, Flat; .125 - .281 - .027
	0400007666	LOCKWASHER, External tooth; #6
	0400007667	LOCKWASHER, External tooth; #4
	0705828F01	BRACKET, Support
	4210217A02	STRAP, Tie

NOTE: For optimum performance, order replacement diodes and transistors by Motorola part number only.



TAPE PLAYER & AMPLIFIER (ASI) SCHEMATIC DIAGRAM



TAPE PLAYER & AMPLIFIER (ASI) CIRCUIT BOARD DETAIL

APPENDIX A
GLOSSARY

ASI - Automatic Station Identification. A recorded station identification message transmitted periodically to satisfy FCC regulations.

ARS - Alternate Receiver Selector. A circuit in the paging terminal that pages a substitute or alternate pager code when the original pager code is dialed.

BULK USER - A subscriber who usually has a large number of units and makes frequent calls to these units. Such a user may be provided a direct line input to terminal equipment eliminating the necessity to dial an outside phone number to access the equipment.

CARRIER CIRCUIT - A connecting path where many different conversations are combined on a single pair of wires or a single radio channel in such a manner as they may take place simultaneously without interfering with each other. This combining is called multiplexing. DC continuity between the parties or equipment at either end does not exist, however, alternate means of signalling may be available.

CO - Central Office. The location of the common switching equipment in the telephone system that connects various lines together to form a connecting path for voice and other forms of information transmission.

CODE TYPE - A pager coding method requiring a prefix letter for each code.

CONNECTOR LEVEL - The connector is the last switch in the chain of central office switches (cf. step-by-step, selector level). It is controlled by the final two digits of a telephone number. It connects the calling party to an individual telephone line and causes ringing voltage to be applied to the line. It is normally <u>not</u> possible to obtain DC dial pulses from a connector level as the calling line is only capacitively coupled to the called line.

CP - Construction Permit. A document issued by the Federal Communications Commission (FCC) allowing the construction of a radio station. This document details the RF design of the system as proposed by the applicant (licensee). No deviations from this design may be made without notifying the Commission. There is a time limit set during which construction must be completed. This limit is normally eight months from the date of initial grant. A three to six month extension may be granted under unusual circumstances.

CS - Control Sleeve. A supervisory lead associated with a telephone exchange (cf. sleeve).

CROSSBAR - A switching system using crossbar switches to make the selection of the called subscriber. Digits are stored in a common control portion of the circuitry and at completion of dialing, a translation takes place and a crash selection occurs.

As dial pulses are stored and not normally repeated in this type of system, it may not be possible to obtain these pulses at a "selector" level interconnection point. Only crossbar central offices equipped for <u>line-link pulsing can</u> provide selector level dial pulsing. There are two common types of crossbar central office designated No. 1 and No. 5.

DDD - Direct Distance Dialing. There may or may not be a special digit(s) required before the long distance telephone number to access the telephone company DDD equipment, e.g., 1, 112, 110.

DTMF - Dual Tone Multiple Frequency. Each digit of a telephone number is represented by two audio tones, a high tone and a low tone. The popular systems use four low tones (697, 770, 852, and 941 Hz) and three high tones (1209, 1336, and 1477 Hz).

END-TO-END - A term often used to designate a type of signalling system where information at one end of the switched telephone network (calling party's phone) is transmitted to the other end of the switched network (called party's phone). This transmission is usually accomplished by sending tones over the circuit.

ESS - A switching system using electronic switches to make the selection of the desired called subscriber. Digits are stored in the common control portion of the circuitry and translated to machine language for selection. The switching in this type of central office is extremely fast as most of the equipment is solid state. This type of central office can best be thought of as a big computer. Several types of ESS offices exist, the most common being Bell's No. 1 and No. 101 and Automatic Electric's EAX.

FULL DUPLEX - Transmitting and receiving (talking and listening) at the same time. A telephone is an example of a full duplex circuit.

FX LINE - Foreign Exchange Line. This is a line to a location from a telephone company central office that does not serve the location. It may be outgoing or incoming or both. This line would be used to provide toll-free service to and/or from a distant location. An example would be a line between a terminal in Miami and a telephone company central office in Fort Lauderdale. A person in Fort Lauderdale could now place a local call and be connected to the Miami terminal.

GRADE OF SERVICE - A measure of what percentage of calls to a given number, selector level, exchange, etc., encounter a busy condition. For example, if 1 call out of every 100 calls got a busy signal, the grade of service would be 1%.

IMTS - Improved Mobile Telephone System.

IMTS SIGNALLING - A digital signalling scheme normally used to call mobiles by alternatively sending an 1800 Hz tone and a 2000 Hz tone. The tone shifts the same number of times as the value of the digit dialed.

KEY (transmitter) - Process of activating the base station transmitter for the purpose of producing rf energy.

LOCAL (transmitter) - Transmitter (base station) located at the same site as the encoder.

LOOP RESISTANCE - The DC resistance measured across a pair of wires. The other end of the pair is either shorted together or terminated in its normal manner by a piece of equipment that has DC continuity.

MAKE-BREAK - The ratio between the open and closed time of contacts on a telephone dial when it is pulsing (dialing). This ratio is normally 60% break - 40% make. In a 10 pps system, this means the line will be open for 60 ms. and closed for 40 ms. The number of times corresponding to the value of the digit dialed.

P.01 - A designation of the grade of service (cf.) of a circuit. P.01 is a 1% grade of service; P.02 is a 2% grade of service, etc.

PABX - Private Automatic Branch Exchange.

PAGER - An fm receiver normally activated only when it receives two specific audio tones in sequence, for a specific duration.

PAGING TERMINAL - A unit that receives the telephone call and pager number, then generates the proper tones for transmission.

PEG COUNT - A digital counting scheme using electro-mechanical counters.

POLARITY GUARD - A circuit installed in a Touch-Tone telephone to allow the sending of tones after the called party has answered. Some central offices cause the battery polarity to the calling telephone to be reversed after the called party has answered. If this occurs and the calling parties phone is not equipped with polarity guard, he will no longer be able to transmit tones thus prohibiting him from entering a page in an end-to-end paging system. Polarity guard will normally be furnished as a no-charge or one-time-charge option by the telephone company, if requested.

PPS - Pulses Per Second. Describes the speed at which dial pulses are sent. A standard telephone dial has a nominal speed of 10 pps. Special dials and equipment may operate at 20 pps.

"PRIVATE-LINE" (PL) - Method of implementing private (or semi-private) communications using a coded PL tone to unsquelch the receiver.

PROM - A programmable ROM.

RAM - Random Access Memory. A memory in which the access time is independent of the locations being addressed. Any location can be addressed directly.

REMOTE (transmitter) - Transmitter located at a remote site and interconnected with the terminal through a remote control console.

RESISTANCE (Battery/Ground) - A resistor of some value is placed in series with the hot lead or the ground lead of a battery (or DC power supply).

REVERSE BATTERY - A type of supervisory indication to telephone company equipment indicating that a telephone has been answered or hung up. This supervision is normally used on a selector level system in a crossbar or ESS office.

RING - One side of a telephone line. It derives its name from switchboard usage where it is normally wired to the insulated middle ring on a plug. It is one side of the audio line. (cf., tip, sleeve).

RINGING VOLTAGE - The AC voltage applied to the telephone line to cause the bell in a telephone to ring. The different types in common usage are as follows:

Harmonic - Frequency Selective ringing 16-2/3 - 25 - 33-1/3 - 50 - 66-2/3 Hz.

Decimonic - Frequency Selective ringing 20 - 30 - 40 - 50 - 60 Hz.

Synchromonic - Frequency Selective ringing 16* - 30 - 42 - 54 - 66 Hz
* or 20

Superimposed - Battery Selective ringing 20 Hz AC on + or - battery.

Coded - Duration/Timing Selective ringing 20 Hz AC of varying duration.

ROM - Read Only Memory. A device that supplies a predetermined binary output, when it receives a given input address. Used to store two-tone frequency information in a paging system.

SEL-CALL RADIO - A two-way radio with a built-in selective call decoder circuit that enables the radio to also function as a pager.

SELECTOR LEVEL - A term generally used to indicate a point in the telephone company's switching system which is common to many numbers. Each of the first five digits of a local seven digit telephone number may be thought of as a selector level. The value of the digit dialed determines how many positions the selector switch moves (cf., step-by-step). For example, if the first digit of a telephone number is a 5 the first selector will step 5 positions and connect the calling line to a second selector; if the second digit is an 8 the second selector will step 8 positions and connect the caller to a third selector, and so on. Thus, a first selector is common to 1,000,000 telephone numbers, the second selector to 100,000 numbers, etc. The table below indicates common interconnection points and the number capability at each one.

Selector Level	Numbers
3rd	10,000
4th	1,000
5th	100

SHARED CHANNEL - The same rf frequency used by two or more radio transmitters.

SLEEVE - A supervisory lead associated with a telephone exchange. It derives its name from switchboard usage where it is connected to the long sleeve portion of a plug. It is used to indicate various conditions to the telephone switching equipment. Some of these conditions are busy, off-hook and on-hook.

STEP-BY-STEP - A telephone switching system that makes a step in the selection process for every digit dialed. The selection process progresses step-by-step until the called party is selected. Much of the step-by-step equipment is based on the two motion switch invented by Strowger. This system was the basis for the early automatic telephone exchanges and is still in wide usage today.

SUBAUDIBLE PAGING - A tone-only signalling system that is superimposed on a system used for other purposes. It does not interfere with a conversation taking place on the system it is using. The subaudible tones are not truly inaudible but are present at a very low level in a mobile radio's speaker.

SUBAUDIBLE PAGING TONES - Audio paging tones in the frequency range below the bandpass of most communications receivers (below 300 Hz).

SYNTHESIZER - A device which generates many output frequencies based on a single stable frequency source. The divider type uses a crystal-controlled master oscillator and outputs are submultiples of the master oscillator.

TIP - One side of a telephone line. It derives its name from switchboard usage where it is normally wired to the tip (or end) lead of the connecting jack or plug. It is one side of the audio line. (cf., ring, sleeve).

TONE AND VOICE PAGER - A pager that provides an alert "beep", followed by a voice message from the caller.

TONE ONLY PAGER - A pager that provides alert beeping only.

TOUCH-TONE® - A registered trademark of the Bell System, for a dual tone multiple frequency (DTMF) signalling (dialing) scheme.

TRANSMITTER CONTROL - Refers to the technique of controlling the paging transmitter. Local control is for transmitters within 50 feet of the terminal. DC control is used for greater (remote) distances.

TWO-TONE SYSTEM - Paging system based on two distinct paging frequencies.

UNI - Universal Number Interchange. (cf. ARS)

USOC CODE - Universal Service Order Code. An abbreviated means of identifying interconnection devices supplied by the telephone company. It usually consists of three to five letters and/or numbers and designates a particular piece of equipment to be used for connecting the telephone companies switched network to a subscriber's equipment. The designator QKT specifies what used to be called a "Model 30 Voice Coupler" which is a device that is employed in phone patch systems. The designator RDL specifies a device equivalent to the K519522L1 recorder coupler used in end-to-end paging systems.

VOICE CONNECTING ARRANGEMENT (DCK/DCW) - An interface circuit for protecting the telephone company selector level telephone line from possible damage due to customer connected equipment.

VOICE CONNECTING ARRANGEMENT (RDMZR) - An interface circuit for protecting the telephone company end-to-end telephone line from possible damage due to customer connected equipment.

X-Y - A type of switching system similar to Strowger switch using a switch manufactured by the Stromberg-Carlson Company. Its action is rectangular instead of vertical and rotary as in a Strowger switch. (cf., step-by-step).

2805 SIGNALLING - A digital signalling scheme normally used to call mobiles by sending a 2805 Hz tone and interrupting it with a dial. The number of the interruptions corresponds to the value at the digit dialed.

APPENDIX B
BASIC LOGIC CIRCUITS

1. GENERAL

Symbolic logic provides a simplified means of presenting a series of events which are controlled by two-state devices. Most logical operations performed by the terminal are accomplished through the use of TTL (transistor-transistor logic) integrated circuits. TTL logic is two-state: high and low where "high" is defined as 5 volts or high impedance and "low" is defined as ground or low impedance. Generally, an active signal is defined as a high signal. The simplest circuit used in the terminal is the inverter circuit which is shown symbolically in Figure 1. The inverter circuit element produces an output which is the inverse of the input; i.e., a logic "high" at the input pin becomes a logic "low" at the output pin and vice versa. A 1 indicates a "high" signal and a 0 indicates a "low" signal.

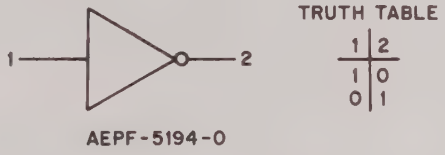


Figure 1. Inverter Circuit

2. GATES

The most basic logic operations involving two or more signals are performed by gating circuits, of which there are several types. Each gate has two or more inputs which correspond to two or more active or inactive input signals. The output can be determined by consulting a "truth table" which lists all combinations of input signals and the resulting output for each combination. The logic symbols and truth tables are shown in Figure 2.

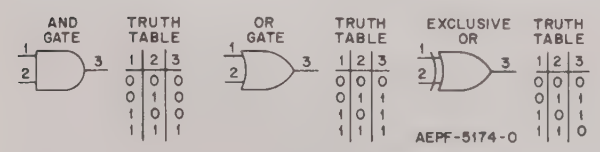


Figure 2. AND/OR Gates

The presence of a circle on a logic symbol indicates the signal is inverted at the circle (a "high" would be changed to a "low" and a "low" would be inverted to a "high"). A circle on the output of an AND gate changes it to a NAND gate. A circle on the output of an OR gate changes it to a NOR gate. A circle on an exclusive-OR gate changes it to an exclusive-NOR gate. These logic symbols and their truth tables are shown in Figure 3. Note that the truth tables are the same as the corresponding tables in Figure 2 except column 3 has the 0 changed to a 1 and the 1 changed to a 0.

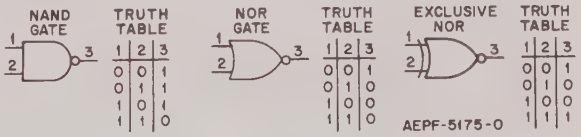


Figure 3. NAND/NOR Gates

Sometimes an active signal may be defined as a "low". This signal may be converted to the more conventional "high" by inverting the signal at the input of the logic symbol. Thus a circle on the input of a logic symbol indicates that the signal, when active, is a "low". The symbols are corresponding truth tables are shown in Figure 4. Note that the negative-OR gate and the truth table for the negative-AND gate is the same as that of the NOR gate.

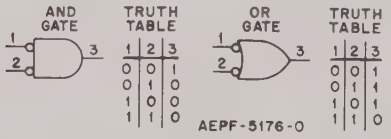


Figure 4. Inverted Inputs

3. RS TYPE FLIP-FLOPS

A simple RS flip-flop, composed of two NAND gates, is shown in Figure 5. The S denotes a "set" input and the R denotes a "reset" input.

The "set" input switches the circuit to the logically active state. The "reset" input returns the circuit to the "non-active" state. The bars above the letters indicate that these inputs are "active low"; that is, these inputs trigger their intended functions when they are at the low logic level (.2 V max.). The outputs are shown in the "set" condition ($\overline{Q}$ low, Q high). Assume that a low $\overline{R}$ input has occurred and the circuit is in the reset condition (Q high, $\overline{Q}$ low). The next low $\overline{S}$ pulse will deactivate gate B producing a high Q output. The Q output will now activate gate A producing a low $\overline{Q}$. The circuit will remain in this condition until the next "reset" pulse is applied at the $\overline{R}$ input. The flip-flop is "storing" an input. When a low pulse is applied at $\overline{R}$, gate A is deactivated and Q goes high. The high Q level activates gate B at this time and the Q output goes low. The circuit is now in the "reset" condition and ready for the next input.

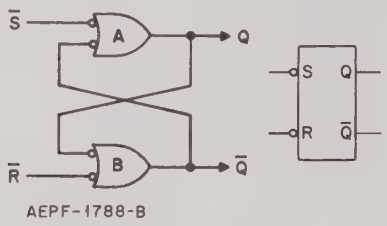


Figure 5. RS Flip-Flop

A fairly simple extension of the RS type flip-flop is produced by the addition of a 2-input NAND gate to both the "set" and "reset" inputs. This addition is shown in Figure 6. One of the inputs to each NAND gate is tied to a common clock or trigger line. A change of state is therefore inhibited until a positive-going clock pulse is applied. This effectively synchronizes the operation of the flip-flop to the clock rate. The truth table is the same as that for the RS flip-flop. For example, assume that a low $\overline{R}$ input has occurred and the circuit is in the reset condition ($\overline{Q}$ high, Q low). The next high $\overline{S}$ pulse will enable gate A so that when the positive-going clock pulse arrives, NAND gate B will deactivate and result in a high Q output. The Q output will now activate gate D, producing a low $\overline{Q}$ output.

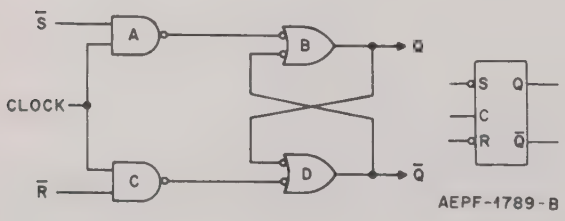


Figure 6. 2-Input RS Flip-Flop

4. D-TYPE FLIP-FLOP

Another clocked flip-flop is the D-type which provides for separate direct set and reset inputs, in addition to the data (D) input and the clock input; see Figure 7. In this circuit, the single-ended D input is connected directly to the gate input (gate A). An inverter is provided between the input line (D) and the reset (R) input. This ensures that the set and reset inputs cannot be high at the same time. The flip-flop employs a 3-input NAND gate on each side of the circuit (gates B and E) to provide for the direct set and reset inputs. Thus, the flip-flop can be set or reset directly, irrespective of the clock input. During the clock transition, the state of the D input is transferred to the Q output, as shown in the truth table. D_N refers to the time at which clock pulse N occurs, while Q_{N+1} refers to the time at which the following clock pulse occurs.

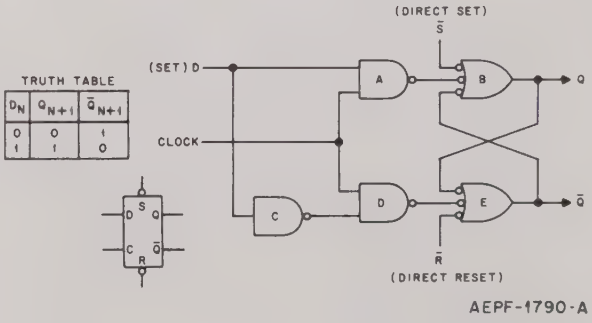
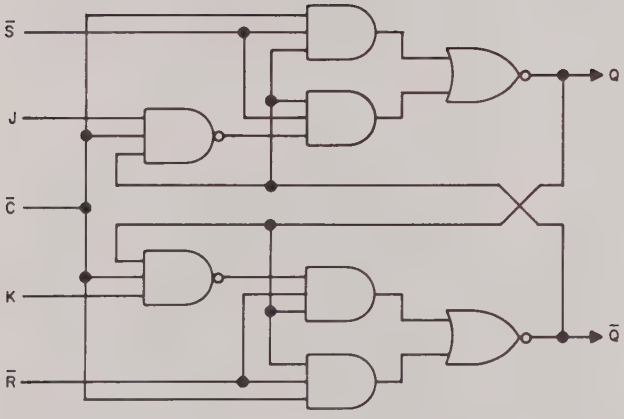


Figure 7. D-Type Flip-Flop

5. J-K TYPE FLIP-FLOP

Still another type of flip-flop used in the terminal is the J-K flip-flop. This type also has direct set and direct reset inputs as described for the D-type flip-flop. However, it has two data inputs which are the so-called J and K inputs. The logic circuit diagram is given in Figure 8. Here, the J-K flip-flop triggers on

the negative edge of the clock input. Data may be applied to or changed at the clocked inputs at any time during the clock cycle, except during the time interval between the setup and hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data states at the inputs throughout the interval between the setup and hold times is stored in the flip-flop when the clock pulse fails. The flip-flop may be set at any time without regard to the clock state by applying a low level to the $\overline{S}$ input. In addition, the flip-flop may be reset by using the $\overline{R}$ input at any time.



TRUTH TABLE

J	K	Q_N	Q_N+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	0	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

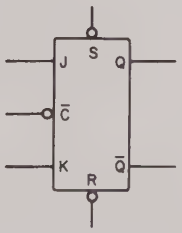


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Figure 8. J-K Flip-Flop

6. RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

The retriggerable monostable multivibrator produces an accurately timed output pulse from either edge of an input pulse. The output pulse width may be varied from 40 nanoseconds to 40 seconds by using appropriate external timing components. Referring to Figure 9, inputs A and B are negative-edge triggered and will trigger the multivibrator into the active state when either or both go low while both C and D are high. The C and D inputs will trigger the multibrator when they both go high while either A or B is low. Triggering occurs at a particular voltage level and is independent of the input pulse transition time. The duration and accuracy of the complementary output pulses (Q and $\overline{Q}$) are determined by the external timing components R_x and C_x. Each time the input conditions for triggering are met, the external timing capacitor (C_x) is discharged, starting a new output pulse. The output goes to the high state while C_x is being discharged and remains there until the capacitor recharges through R_x to a threshold determined by an internal comparator. Input pulses applied during the active state again discharge the capacitor, thus adding another full timing cycle to the output pulse width. For applications where retriggering is not required, appropriate feedback from the outputs (shown by the dotted lines) will inhibit trigger pulses arriving during the active timing cycle.

TRUTH TABLE

A	B	C,D	Q
1	1	1	0
0	X	0	0
X	0	0	0
0	X	1	1
X	0	1	1
X	1	0	0
1	X	0	0

X = DO NOT CARE

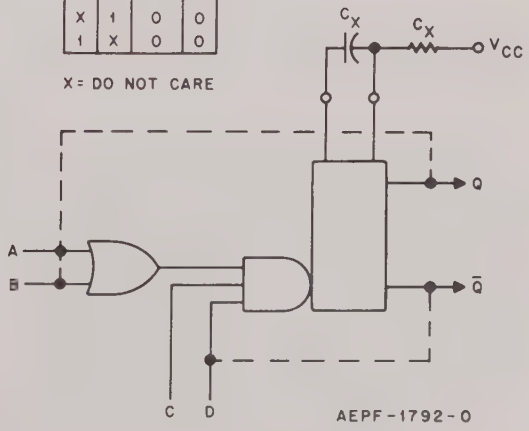

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Figure 9. Retriggerable Multivibrator

7. 4-BIT BINARY COUNTER

The 4-bit binary counter consists of four clocked flip-flops connected to provide a divide-by-16 function; i. e., the counter counts in straight binary (ripple) fashion. Connections to the counter are made so that the Q output of each flip-flop drives the clock (C) input of the following flip-flop. Thus, each time a flip-flop is reset, the Q output falls and triggers the following flip-flop into the set state. The logic diagram given in Figure 10 and the accompanying truth table and timing diagram illustrate the straight binary operation of the counter. When the count reaches 15, all flip-flops are reset by the next clock pulse and the count "rolls over" to zero. A common gated reset input (R) is provided to preset the counter to the zero state (count 0) at any time.

COUNTING SEQUENCE TRUTH TABLE

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

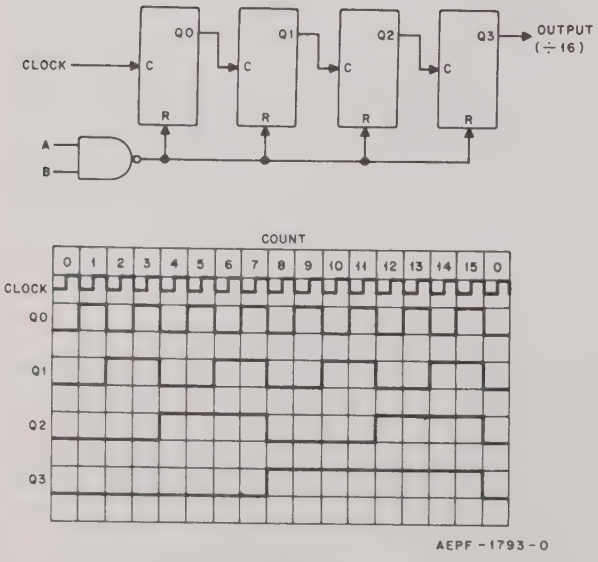


Figure 10. 4-Bit Counter

8. PRESETTABLE 4-BIT BINARY COUNTER

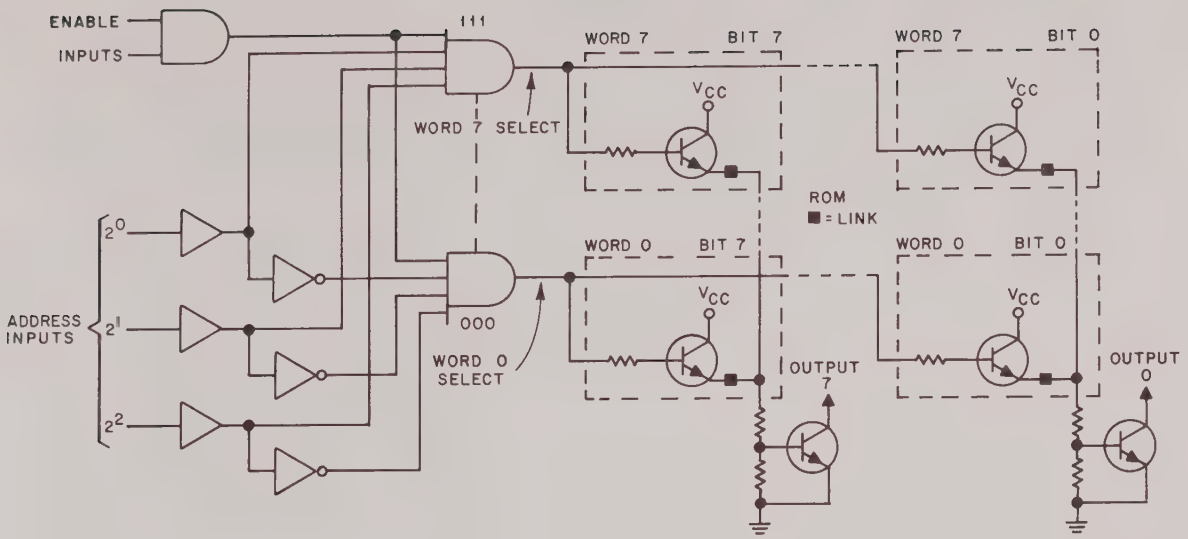
The presettable 4-bit binary counter consists of four clocked J-K flip-flops connected to provide a divide-by-16 function; i. e., the counter counts in a straight binary fashion as described for the 4-bit binary counter in Figure 10. However, this counter also contains additional parallel inputs for presetting data into the counter and parallel outputs for full counting flexibility. Parallel information may be preset only while the parallel enable signal at pin 9 is in the logic 0 state.

Four of these counters are used in the 16-bit tone synthesizer of the terminal output unit. Here, a 16-bit preset word is applied to the parallel inputs ($2^0 \ldots 2^3$) of each of the four counters to shorten the time required to reach the full count. In operation, a stable oscillator clocks the counter and when the full count is reached, the counter logic produces a change of state in the output and begins the count at the preset value. The output from the overall counter, therefore, is a continuous squarewave at a fraction of the oscillator frequency. The counting sequence truth table and timing diagram for the presettable counter are the same as that given in Figure 10 for the 4-bit binary counter.

9. ONE-OF-EIGHT DECODER

The one-of-eight decoder consists of a 64-bit read-only memory (ROM), capable of holding eight 8-bit words, and appropriate address decoding and readout control gating logic. A 3-bit binary input address selects the desired word for the 8-bit output. A separate 2-input AND gate is also provided for enabling the network of address decoding gates. The truth table shown in Figure 11 indicates the contents of each 8-bit word and its associated 3-bit address. The ROM consists essentially of an array of 64 emitter followers, arranged in an 8-by-8 matrix, and a set of eight readout transistors; see Figure 11.

In operation, when a particular address has been decoded, a full column of eight transistors will be turned on. The positive voltage then present at each emitter will turn on the associated readout transistor if the metalization link is in place; i. e., a logic 1 is transferred to the emitter of each readout transistor where the link is in place, but a logic 0 is transferred where the link is removed. Thus, the ROM can be programmed once to readout the words shown in the truth table and this will remain fixed unless the metalization links are changed.



TRUTH TABLE

ADDRESS IN			OUTPUT							
2^2	2^1	2^0	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

AEPF-1794-0

Figure 11. One-of-Eight Decoder

NOTES

APPENDIX C
INTEGRATED CIRCUIT PACKAGES

Data sheets of all the integrated circuit packages used in the paging encoder are present in this appendix. The packages are grouped according to manufacturer and then illustrated in sequence by type number. These numbers correspond to those shown on the schematic diagram.

TYPE		PAGE
Motorola MC3302,	Quad Comparator	C-2
Motorola MC3303,	Quad Differential Input Op Amp	C-3
Motorola MC3380,	Emitter Coupled Astable Multivibrator	C-4
Motorola MC3403,	Quad Differential Input Op Amp	C-3
Motorola MC7708,	Positive Voltage Regulator (750 mA)	C-5
Motorola MC78L08,	Positive Voltage Regulator (100 mA)	C-6
Motorola MC14001,	Quad Two-Input NOR Gate	C-7
Motorola MC14002,	Dual Four-Input NOR Gate	C-8
Motorola MC14011,	Quad Two-Input NAND Gate	C-9
Motorola MC14013,	Dual Type D Flip-Flop	C-10
Motorola MC14015,	Dual Four-Bit Static Shift Register	C-11
Motorola MC14016,	Quad Analog Switch/Quad Multiplexer	C-12
Motorola MC14017,	Decade Counter/Divider	C-13
Motorola MC14024,	Seven-Stage Ripple Counter	C-14
Motorola MC14027,	Dual J-K Flip-Flop	C-15
Motorola MC14028,	BCD-to-Decimal/Binary-to-Octal Decoder	C-16
Motorola MC14040,	12-Bit Binary Counter	C-17
Motorola MC14049,	Hex Inverter/Buffer	C-18
Motorola MC14052,	Analog Multiplexers/Demultiplexers	C-19
Motorola MC14069,	Hex Inverter	C-20
Motorola MC14069,	Hex Inverter	C-17
Motorola MC14071,	Quad Two-Input OR Gate	C-18
Motorola MC14073,	Triple Three-Input AND Gate	C-19
Motorola MC14075,	Triple Three-Input OR Gate	C-20
Motorola MC14081,	Quad Two-Input AND Gate	C-21
Motorola MC14175,	Quad Type D Flip-Flop	C-22
Motorola MC14419,	2-of-8 Keypad-to-Binary Encoder	C-23
Motorola MC14503,	Hex Three-State Buffer	C-24
Motorola MC14507,	Quad Exclusive OR Gate	C-25
Motorola MC14511,	BCD-to-Seven Segment Latch/Decoder/Driver	C-26
Motorola MC14518,	Dual BCD Up Counter	C-27
Motorola MC14519,	Four-Bit AND/OR Selector	C-28
Motorola MC14520,	Dual Binary Up Counter	C-27
Motorola MC14527,	BCD Rate Multiplier	C-29
Motorola MC14528,	Dual Retriggerable/Resettable Monostable Multivibrator	C-30
Motorola MC14532,	Eight-Bit Priority Encoder	C-31
Motorola MC14572,	Hex Gate	C-32
Motorola MC14584,	Hex Schmitt Trigger	C-33
Motorola 4N25,	Infrared LED Phototransistor Coupled Pair	C-34
Motorola 4N27,	Infrared LED Phototransistor Coupled Pair	C-34
General Instrument	ER3401, 4096 Electrically Alterable ROM	C-35
Harris HM1-0186,	Commercial Diode Matrix (8 x 6)	C-37
National LM380,	Audio Power Amplifier	C-39
Signetics NE555,	Timer	C-43
Signetics NE556,	Dual Timer	C-44

ORDERING INFORMATION

Device	Temperature Range	Package
MC3302L	−55°C to +125°C	Ceramic DIP
MC3302P	−40°C to +85°C	Plastic DIP

MC3302P

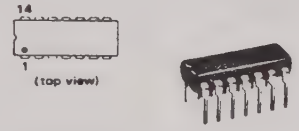
QUAD SINGLE-SUPPLY COMPARATOR

These comparators are designed specifically for single positive-power-supply Consumer Automotive and Industrial electronic applications. Each MC3302P contains four independent comparators – suiting it ideally for usages requiring high density and low-cost.

- Wide Operating Temperature Range – -40 to +85°C
- Single-Supply Operation – +2.0 to +28 Vdc
- Differential Input Voltage = $\pm V_{CC}$
- Compare Voltages at Ground Potential
- MTTL Compatible
- Low Current Drain – 700 μA typical @ V_{CC} +5.0 to +28 Vdc
- Outputs can be Connected to Give the Implied AND Function

QUAD COMPARATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Range	V_{CC}	+2.0 to +28	Vdc
Output Sink Current (See Note 1)	I_O	20	mA
Differential Input Voltage	V_{IDR}	$\pm V_{CC}$	Vdc
Common-Mode Input Voltage Range (See Note 2)	V_{ICR}	-0.3 to +V_{CC}	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	625 5.0	mW mW/°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1. Requires an external resistor, R_L, to limit current below maximum rating.

Note 2. If either (+) or (−) inputs of any comparator go more than several tenths of a volt below ground, a parasitic transistor turns "on" causing high input current and possible faulty outputs.

FIGURE 1 – EQUIVALENT CIRCUIT

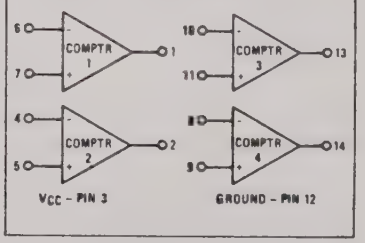
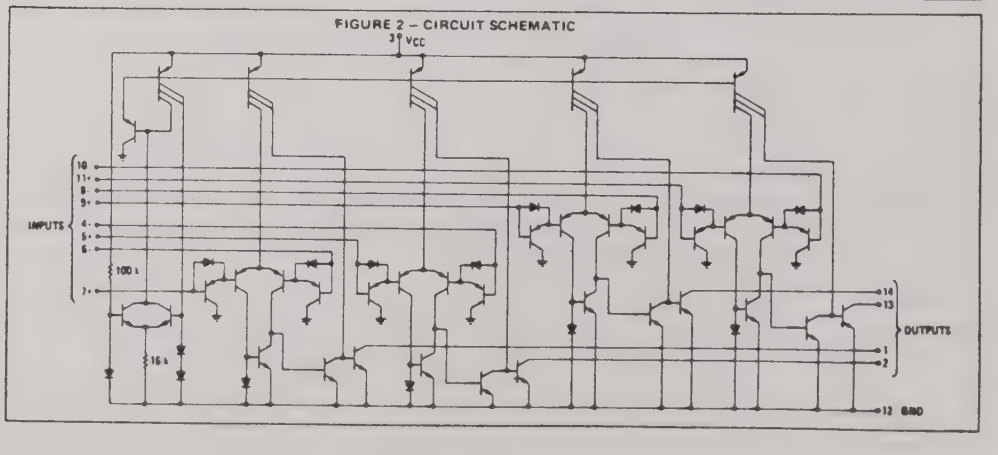


FIGURE 2 – CIRCUIT SCHEMATIC



ORDERING INFORMATION

Device	Temperature Range	Package
MC3303L	−40°C to +85°C	Ceramic DIP
MC3303P	−40°C to +85°C	Plastic DIP
MC3403L	0°C to +70°C	Ceramic DIP
MC3403P	0°C to +70°C	Plastic DIP
MC3503L	−55°C to +125°C	Ceramic DIP

MC3403P,L
MC3503L
MC3303P,L

Specifications and Applications Information

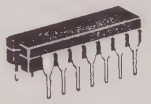
QUAD LOW POWER OPERATIONAL AMPLIFIERS

The MC3503 is a low-cost, quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular MC1741. However, the MC3503 has several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 Volts or as high as 36 Volts with quiescent currents about one third of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

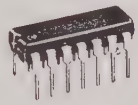
- Short Circuit Protected Outputs
- Class AB Output Stage for Minimal Crossover Distortion
- True Differential Input Stage
- Single Supply Operation: 3.0 to 36 Volts
- Split Supply Operation: ±1.5 to ±18 Volts
- Low Input Bias Currents: 500 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- Similar Performance to Popular MC1741

QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

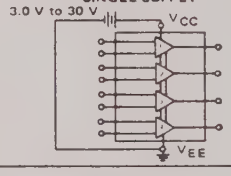


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

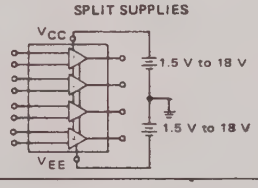


P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC3403 and MC3303 only)

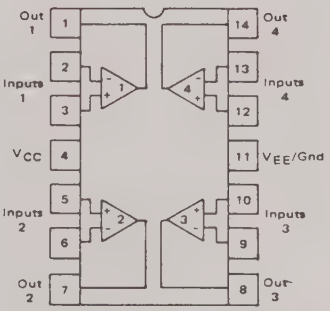
SINGLE SUPPLY



SPLIT SUPPLIES



PIN CONNECTIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC} V_{EE}	 36 +18 -18	Vdc
Input Differential Voltage Range (1)	V_{IDR}	±30	Vdc
Input Common Mode Voltage Range (1) (2)	V_{ICR}	±15	Vdc
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 -65 to +150 -55 to +125	°C
Operating Ambient Temperature Range MC3503 MC3403 MC3303	T_A	 -55 to +125 0 to +70 -40 to +85	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C

(1) Split Power Supplies.
(2) For Supply Voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

ORDERING INFORMATION

Device	Temperature Range	Package
MC3380P	0°C to +75°C	Plastic DIP

MC3380P

EMITTER COUPLED
ASTABLE
MULTIVIBRATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT

EMITTER COUPLED ASTABLE MULTIVIBRATOR
With Programmable Pulse Width and Current-Controlled Pulse Repetition Rate

The MC3380P is a monolithic device designed for use as a general building block in control and power supply applications.

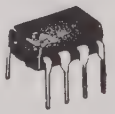
Its extremely flexible design makes it useful in dc-dc converter applications and power supply regulator circuits. Its fixed pulse width, variable frequency mode of operation makes it useful in switching regulator applications with either fixed or variable loads. This device is capable of stepping up (Figures 5 and 9) or stepping down (Figure 14) dc input voltages, and can produce regulated multiple output dc voltages of either positive or negative polarity (Figure 14).

This device can also be used as a frequency source when configured as a multivibrator.

As a DC-DC Converter –
Differential Line Regulation (Figure 9) –
= 1 V (Max) @ V_{CC} = 3 to 7.5 V

As a Power Regulator –
Load Regulation (Figure 5) –
0.2% (Typ) @ P_D = 1 to 3 Watts

As a Multivibrator –
High Toggle Frequency = 100 kHz (Typ)



PLASTIC PACKAGE
CASE 626

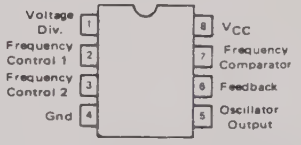
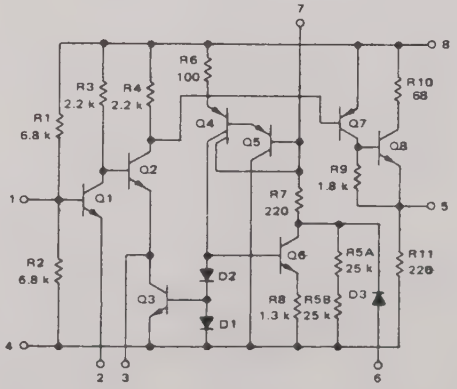


FIGURE 1 – CIRCUIT SCHEMATIC



MC7700C series

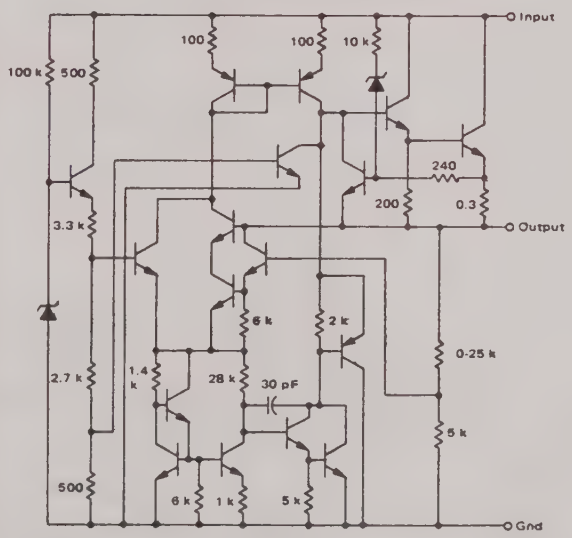
MC7700C SERIES THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC7700C Series positive voltage regulators are identical to the popular MC7800C Series devices, except that they are specified for only half the output current. Like the MC7800C devices, the MC7700C three-terminal regulators are intended for local, on-card voltage regulation.

Internal current limiting, thermal shutdown circuitry and safe-area compensation for the internal pass transistor combine to make these devices remarkably rugged under most operating conditions. Maximum output current, with adequate heatsinking is 750 mA.

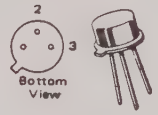
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 313 and Case 79 (TO-220 and Hermetic TO-39)

REPRESENTATIVE SCHEMATIC DIAGRAM



THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

G SUFFIX
METAL PACKAGE
CASE 79
TO-39



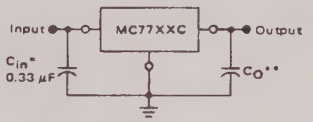
Pin 1. Input
2. Output
3. Ground

Case connected to Pin 3.

T SUFFIX
PLASTIC PACKAGE
CASE 313
(TO-220 Type)

Pin 1. Input
2. Ground
3. Output

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

ORDERING INFORMATION		
DEVICE	TEMPERATURE RANGE	PACKAGE
MC77XXCG	T_J = 0° C to +150°C	Metal Can
MC77XXCT	T_J = 0° C to +150°C	Plastic Power
XX indicates nominal voltage		

TYPE NO./VOLTAGE

MC7705C	5.0 Volts
MC7706C	6.0 Volts
MC7708C	8.0 Volts
MC7712C	12 Volts
MC7715C	15 Volts
MC7718C	18 Volts
MC7720C	20 Volts
MC7724C	24 Volts

MC78L00C,AC Series

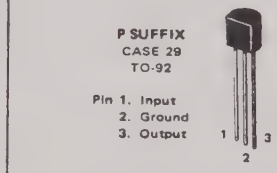
THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

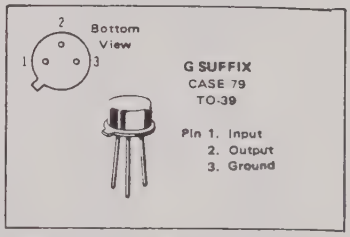
The MC78L00 Series of positive voltage regulators are inexpensive, easy-to-use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

These devices offer a substantial performance advantage over the traditional zener diode-resistor combination. Output impedance is greatly reduced and quiescent current is substantially reduced.

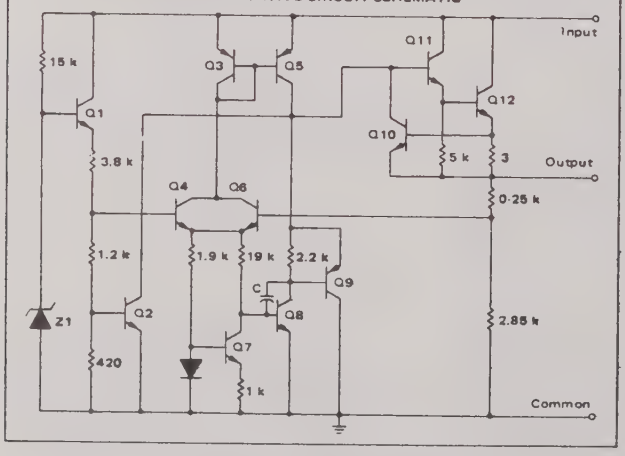
- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

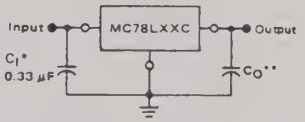




REPRESENTATIVE CIRCUIT SCHEMATIC



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_I is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

Device No. ·10%	Device No. :5%	Nominal Voltage
–	MC78L02AC	2.6
MC78L05C	MC78L05AC	5.0
MC78L08C	MC78L08AC	8.0
MC78L12C	MC78L12AC	12
MC78L15C	MC78L15AC	15
MC78L18C	MC78L18AC	18
MC78L24C	MC78L24AC	24

ORDERING INFORMATION

Device	Temperature Range	Package
MC78LXXACG	T_J = 0°C to +150°C	Metal Can
MC78LXXACP	T_J = 0°C to +150°C	Plastic Transistor
MC78LXXCG	T_J = 0°C to +150°C	Metal Can
MC78LXXCP	T_J = 0°C to +150°C	Plastic Transistor

XX indicates nominal voltage

"NOR" GATE

MC14001AL
MC14001CL
MC14001CP

QUAD 2-INPUT "NOR" GATE

The MC14001 quad 2-Input NOR gate is constructed with MOS P-channel and N-channel enhnacement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14001AL)
  = 3.0 Vdc to 16 Vdc (MC14001CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4001A

McMOS

(LOW POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NOR" GATE

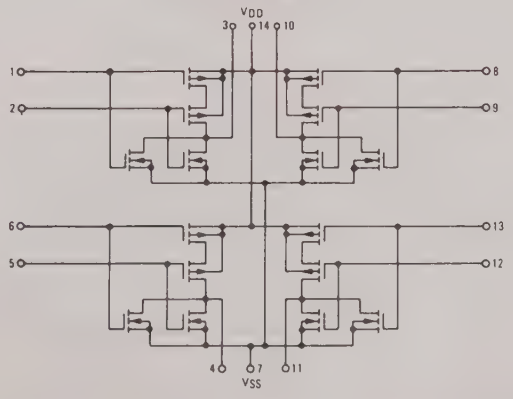
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

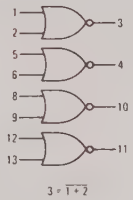
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14001AL MC14001CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14001AL MC14001CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



LOGIC DIAGRAM
POSITIVE LOGIC



$3 = \overline{1+2}$

V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14002AL
MC14002CL
MC14002CP

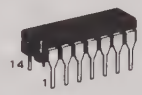
DUAL 4-INPUT "NOR" GATE

The MC14002 dual 4-input NOR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

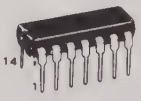
- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14002AL)
  = 3.0 Vdc to 16 Vdc (MC14002CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4002A

McMOS
(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

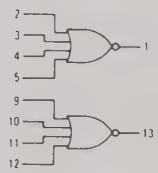


P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating		Symbol	Value	Unit
DC Supply Voltage	– MC14002AL – MC14002CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14002AL – MC14002CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

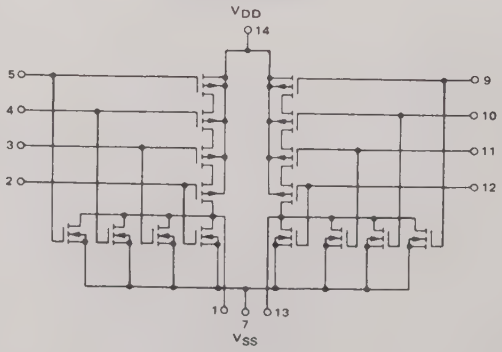
LOGIC DIAGRAM
POSITIVE LOGIC



$1 = \overline{2+3+4+5}$

V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATIC



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14011AL
MC14011CL
MC14011CP

QUAD 2-INPUT "NAND" GATE

The MC14011 quad 2-input NAND gate finds primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14011AL)
  3.0 Vdc to 16 Vdc (MC14011CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4011A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" GATE

L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

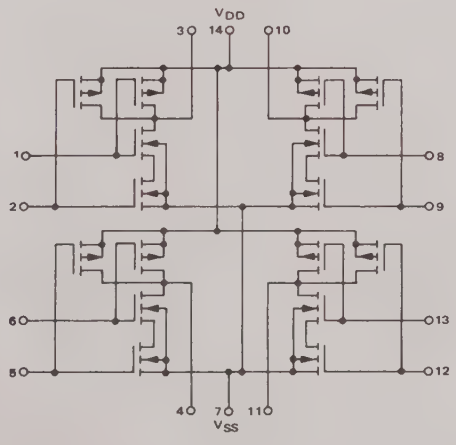
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14011AL MC14011CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14011AL MC14011CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

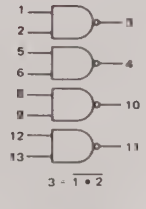
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CIRCUIT SCHEMATIC



LOGIC DIAGRAM
POSITIVE LOGIC



$3 = \overline{1 \bullet 2}$

V_{DD} = Pin 14
V_{SS} = Pin 7

MC14013AL
MC14013CL
MC14013CP

DUAL TYPE D FLIP-FLOP

The MC14013 dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\bar{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Quiescent Power Dissipation = 5.0 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14013AL)
  = 3.0 Vdc to 16 Vdc (MC14013CL/CP)
- Single Supply Operation
- Toggle Rate = 10 MHz
- Logic Edge-Clocked Flip-Flop Design –
  Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse.
- Pin-for-Pin Replacement for CD4013A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL TYPE D FLIP-FLOP

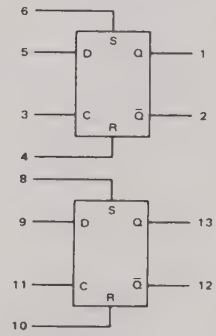
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating	Symbol	Value	Unit
DC Supply Voltage MC14013AL MC14013CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – MC14013AL – MC14013CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

TRUTH TABLE

INPUTS				OUTPUTS		
CLOCK†	DATA	RESET	SET	Q	$\bar{Q}$	
⌐⌐	0	0	0	0	1	
⌐⌐	1	0	0	1	0	
⌐⌐	X	0	0	Q	$\bar{Q}$	No Change
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

X = Don't Care
† = Level Change

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14015AL
MC14015CL
MC14015CP

DUAL 4-BIT STATIC SHIFT REGISTER

The MC14015 dual 4-bit static shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of two identical, independent 4-stage serial-input/parallel-output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register stages are type D master-slave flip-flops. Data is shifted from one stage to the next during the positive-going clock transition. Each register can be cleared when a high level is applied on the Reset line. These complementary MOS shift registers find primary use in buffer storage and serial-to-parallel conversion where low power dissipation and/or noise immunity is desired.

- Quiescent Power Dissipation = 2.5 μW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14015AL)
  = 3.0 Vdc to 16 Vdc (MC14015CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout – >50
- Input Impedance = 10^{12} ohms typical
- Low Input Capacitance – 5.0 pF typical
- Logic Swing Independent of Fanout
- Toggle Rate = 6.0 MHz @ 10 Vdc
- Logic Edge-Clocked Flip-Flop Design –
  Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse.

McMOS

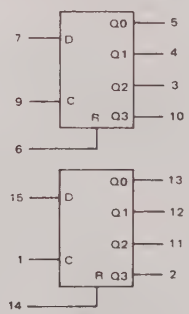
(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-BIT STATIC
SHIFT REGISTER

L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14014AL MC14015CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range – MC14015AL – MC14015CL/CP		T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLES

CLOCKED OPERATION
(SYNCHRONOUS)

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$Q_{n+1} = D_n$, R = 0

DIRECT OPERATION
(ASYNCHRONOUS)

R	Q
0	Q
1	0

C = D = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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MC14016B

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

The MC14016 quad bilateral switch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each MC14016 consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

- High On/Off Output Voltage Ratio – 65 dB Typical
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Low Crosstalk Between Switches – 80 dB typical @ 1.0 MHz
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Transmits Frequencies Up to 54 MHz @ 5 Vdc
- Linearized Transfer Characteristics
- Low Noise – 12nV/$\sqrt{\text{Cycle}}$, f ≥ 1 kHz typical
- Pin-for-Pin Replacement for CD4016, CD4066

McMOS SSI
(LOW-POWER COMPLEMENTARY MOS)

QUAD ANALOG SWITCH
QUAD MULTIPLEXER

L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

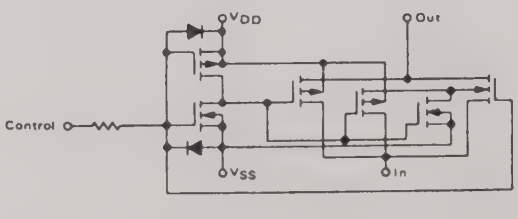
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

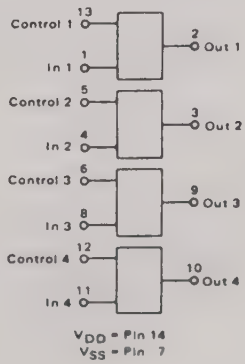
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the control inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} and V_{out} is not constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

CIRCUIT SCHEMATIC
(1/4 OF DEVICE SHOWN)



BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

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MC14017B

McMOS MSI

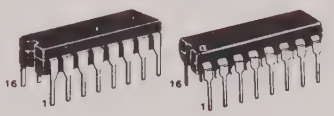
(LOW-POWER COMPLEMENTARY MOS)

DECADE COUNTER/DIVIDER

DECADE COUNTER/DIVIDER

The MC14017B is a five-stage Johnson decade counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- 12 MHz (typical) Operation @ V_{DD} = 10 Vdc
- Divide-by-N Counting
- Quiescent Current = 5.0 nA/package Typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4017



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

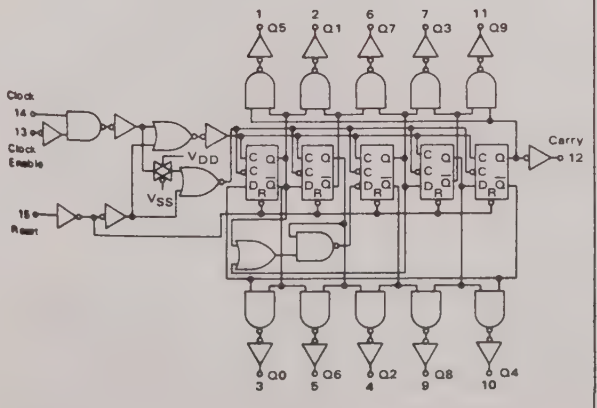
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FUNCTIONAL TRUTH TABLE
(Positive Logic)

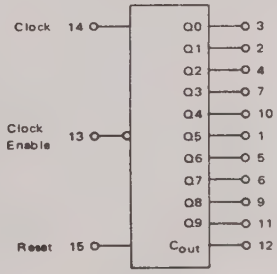
CLOCK	CLOCK ENABLE	RESET	DECODE OUTPUT = n
0	X	0	n
X	1	0	n
X	X	1	Q0
⎍	0	0	n+1
⎍	X	0	n
X	⎎	0	n
1	⎎	0	n+1

X = Don't Care If n < 5 Carry = "1", Otherwise = "0"

LOGIC DIAGRAM



BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

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MC14024B

McMOS SSI

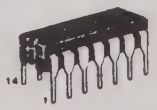
(LOW POWER COMPLEMENTARY MOS)

SEVEN STAGE
RIPPLE COUNTER

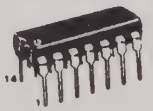
SEVEN STAGE RIPPLE COUNTER

The MC14024B is a seven stage ripple counter with short propagation delays and high maximum clock rates. The Reset input has standard noise immunity (typically 45% of V_{DD}), however the Clock input has a typical noise immunity of 70% of V_{DD} with no maximum Clock input rise or fall time. The output of each counter stage is buffered.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Output Transitions Occur on the Falling Edge of the Clock Pulse
- 8-MHz Operation @ V_{DD} = 10 Vdc typical
- Exceedingly Slow Input Transition Rates may be Applied to the Clock Input
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4024



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

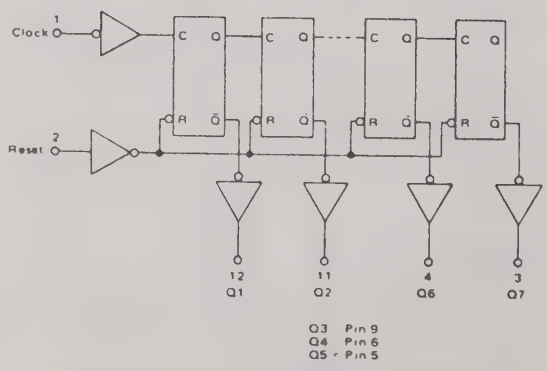
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

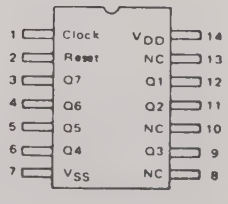
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



Q3 = Pin 9
Q4 = Pin 6
Q5 = Pin 5

PIN ASSIGNMENT



V_{DD} = Pin 14
V_{SS} = Pin 7

NC = No Connection

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MC14027B

DUAL J-K FLIP-FLOP

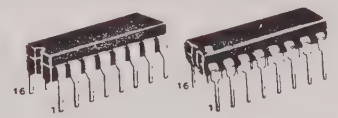
The MC14027B dual J-K flip-flop has independent J, K, Clock (C), Set (S) and Reset (R) inputs for each flip-flop. These devices may be used in control, register, or toggle functions.

- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- Toggle Rate = 3.0 MHz typical @ 5 Vdc
- Logic Swing Independent of Fanout
- Logic Edge-Clocked Flip-Flop Design – Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4027

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL J-K FLIP-FLOP



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

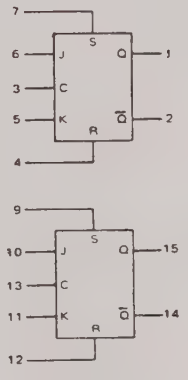
TRUTH TABLE

INPUTS						OUTPUTS*		
C↑	J	K	S	R	Q_n‡	Q_{n+1}	$\overline{Q_{n+1}}$	
⎍	1	X	0	0	0	1	0	
⎍	X	0	0	0	1	1	0	
⎍	0	X	0	0	0	0	1	
⎍	X	⎍	0	0	1	0	1	
⎎	X	X	0	0	X	Q_n	$\overline{Q_n}$	No Change
X	X	X	1	0	X	1	0	
X	X	X	0	1	X	0	1	
X	X	X	1	1	X	1	1	

X = Don't Care
↑ = Level Change
‡ = Present State
* = Next State

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MC14028AL
MC14028CL
MC14028CP

BCD-TO-DECIMAL DECODER
BINARY-TO-OCTAL DECODER

The MC14028 decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one-of-ten) decoded output, while a 3-bit binary input provides a decoded octal (one-of-eight) code output with D forced to a logic "0". Expanded decoding such as binary-to-hexadecimal (one-of-16), etc., can be achieved by using other MC14028 devices. The part is useful for code conversion, address decoding, memory selection control, demultiplexing, or readout decoding.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- High Fanout – > 50
- Buffered Outputs Compatible with HTL and Low-Power TTL
- Positive Logic Design
- Low Power Dissipation of 25 nW/package typical @ V_{DD} = 5.0 V
- Low Outputs on All Illegal Input Combinations
- Pin-for-Pin Replacement for CD4028A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-DECIMAL DECODER
BINARY-TO-OCTAL DECODER

L SUFFIX
CERAMIC PACKAGE
CASE 620

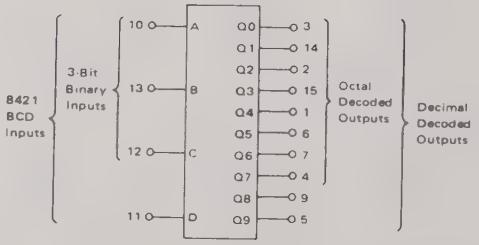
P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage – MC14028AL – MC14028CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - MC14028AL - MC14028CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

INPUT				OUTPUT									
D	C	B	A	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	■	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	■	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	■	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	■	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	■	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

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MC14040B

12-BIT BINARY COUNTER

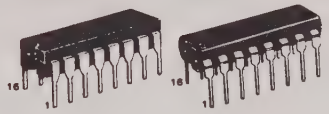
The MC14040B 12-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

- Fully Static Operation
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance = 5.0 pF typical
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Common Reset Line
- 13 MHz Typical Counting Rate @ V_{DD} = 15 V
- Pin-for-Pin Replacement for CD4040

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

12-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

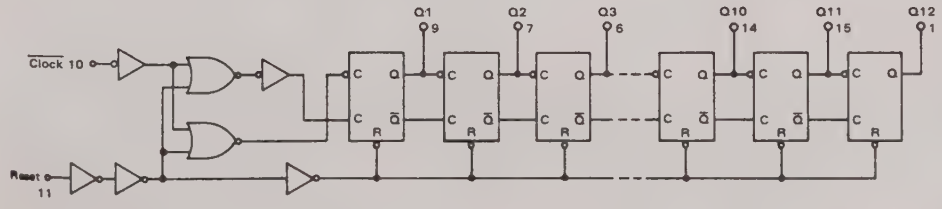
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
↑	0	No Change
↓	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM



Q4 = Pin 5 Q7 = Pin 4
Q5 = Pin 3 Q8 = Pin 13
Q6 = Pin 2 Q9 = Pin 12

V_{DD} = Pin 16
V_{SS} = Pin 8

MC14049AL
MC14049CL
MC14049CP
MC14050AL
MC14050CL
MC14050CP

HEX BUFFERS

The MC14049 hex inverter/buffer and MC14050 noninverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, V_{CC}. The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage for logic-level conversions. Two TTL/DTL loads can be driven when the devices are used as CMOS-to-TTL/DTL converters (V_{CC} = 5.0 V, $V_{OL} \leq$ 0.4 V, $I_{OL} \geq$ 3.2 mA). Note that pin 16 is not connected internally on these devices; consequently connections to this terminal will not affect circuit operation.

- Direct Drive of Two TTL/DTL Loads
- High Source and Sink Currents
- High-to-Low or Low-to-High Level Converter
- Quiescent Power Dissipation = 5 nW/package typical @ 5 Vdc
- Single-Supply, Pin-for-Pin Replacements for Types MC14009 and MC14010 Respectively

McMOS

(LOW POWER COMPLEMENTARY MOS)

HEX BUFFERS

Inverting — MC14049AL/CL/CP
Noninverting — MC14050AL/CL/CP

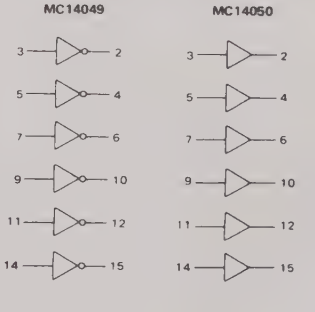
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	AL Version	V_{CC}	+18 to -0.5	Vdc
	CL,CP Version		+16 to -0.5	
Input Voltage, All Inputs		V_{in}	+18 to -0.5	Vdc
DC Current per Input Pin		I_{in}	10	mAdc
DC Current per Output Pin		I_{out}	45	mAdc
Operating Temperature Range	AL Version	T_A	-55 to +125	°C
	CL,CP Version		-40 to +85	
Storage Temperature Range		T_{stg}	-65 to +150	°C
Maximum Dissipation per Package		P_D	See Figure 1	

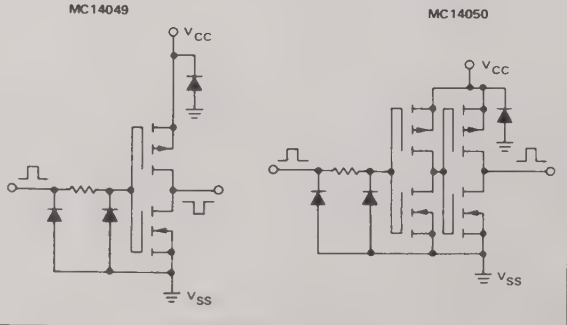
LOGIC DIAGRAMS



NC = Pin 13, 16
V_{SS} = Pin 8
V_{CC} = Pin 1

NC = Pin 13, 16
V_{SS} = Pin 8
V_{CC} = Pin 1

CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

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MC14051B
MC14052B
MC14053B

ANALOG MULTIPLEXERS/DEMULTIPLEXERS

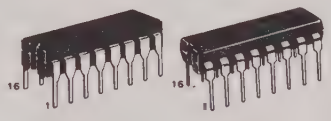
The MC14051, MC14052 and MC14053 analog multiplexers are digitally controlled analog switches. The MC14051 effectively implements an 8PST electronic switch, the MC14052 a 4PDT, and the MC14053 a DP3T. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- High On/Off Output Voltage Ratio — 65 dB typical
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Crosstalk Between Switches — 80 dB typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Transmits Frequencies Up to 65 MHz
- Linearized Transfer Characteristics, $\Delta R_{ON} < 60\ \Omega$ for $V_{in} = V_{DD}$ to V_{EE} @ 15 Vdc
- Low Noise — 12 $nV/\sqrt{Cycle}$, $f \geq 1$ kHz typical
- Pin-for-Pin Replacement for CD4051, CD4052, and CD4053

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXERS/ DEMULTIPLEXERS



CASE 620
L SUFFIX
CERAMIC PACKAGE

CASE 648
P SUFFIX
PLASTIC PACKAGE

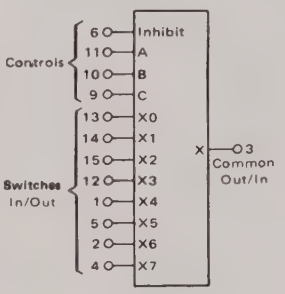
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

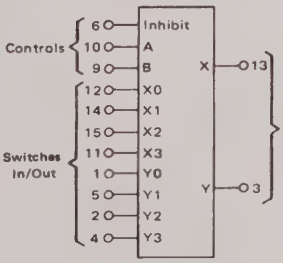
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	25	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

MC14051
8-Channel Analog Multiplexer/Demultiplexer



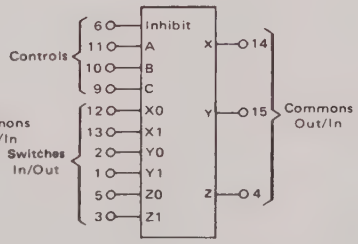
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

MC14052
Dual 4-Channel Analog Multiplexer/Demultiplexer



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

MC14053
Triple 2-Channel Analog Multiplexer/Demultiplexer



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

Note: Control Inputs referenced to V_{SS}. Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be $\leq V_{SS}$.

TRUTH TABLE

Control Inputs				ON Switches		
	Select					
Inhibit	C*	B	A	MC14051	MC14052	MC14053
0	0	0	0	X0	Y0 X0	Z0 Y0 X0
0	0	0	1	X1	Y1 X1	Z0 Y0 X1
0	0	1	0	X2	Y2 X2	Z0 Y1 X0
0	0	1	1	X3	Y3 X3	Z0 Y1 X1
0	1	0	0	X4		Z1 Y0 X0
0	1	0	1	X5		Z1 Y0 X1
0	1	1	0	X6		Z1 Y1 X0
0	1	1	1	X7		Z1 Y1 X1
1	x	x	x	None	None	None

*Not applicable for MC14052
x Don't Care

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MC14069B

HEX INVERTER

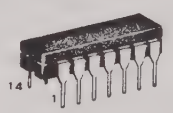
The MC14069B hex inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4069B

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX INVERTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

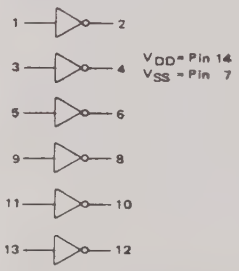
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ORDERING INFORMATION

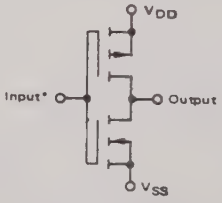
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)

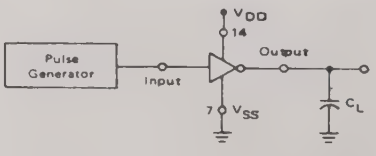


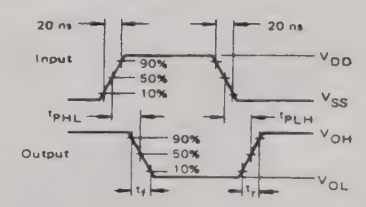
*Double diode protection on all inputs not shown.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





MC14071AL
MC14071CL
MC14071CP

QUAD 2-INPUT "OR" GATE

The MC14071 quad 2-input OR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14071AL)
  = 3.0 Vdc to 16 Vdc (MC14071CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout

McMOS

(LOW POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "OR" GATE

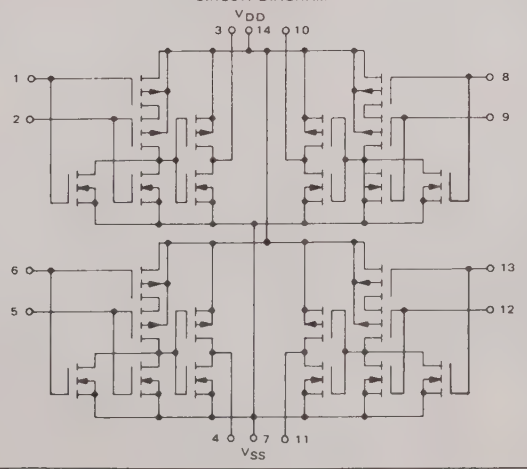
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7.)

Rating		Symbol	Value	Unit
DC Supply Voltage	–MC14071AL –MC14071CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14071AL – MC14071CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

CIRCUIT DIAGRAM



LOGIC DIAGRAM

3 - 1 + 2

V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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MC14073B

B-SUFFIX SERIES McMOS GATES

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4073B

McMOS SSI

(LOW POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "AND" GATE

L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

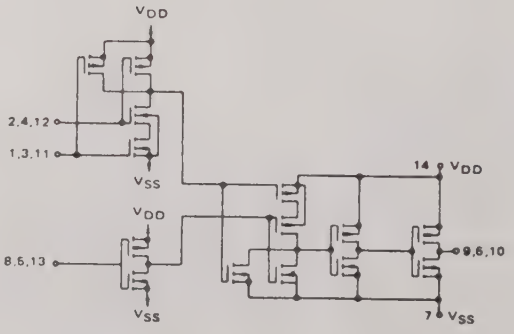
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

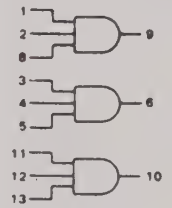
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATICS
(1/3 of Device Shown)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA Semiconductors

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MC14075B

B-SUFFIX SERIES McMOS GATES

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

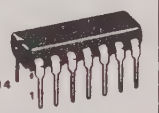
- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4075B

McMOS SSI

(LOW POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "OR" GATE

L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

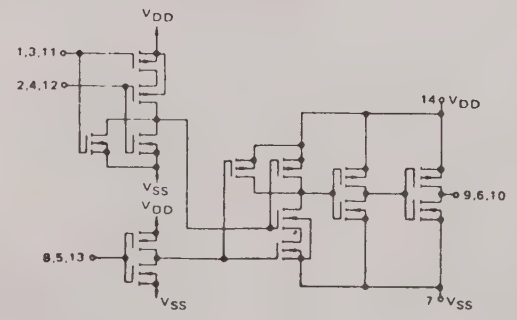
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

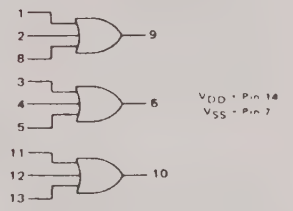
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATIC
(1/3 of Device Shown)



LOGIC DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14081AL
MC14081CL
MC14081CP

QUAD 2-INPUT "AND" GATE

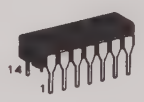
The MC14081 quad 2-Input AND gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14081AL)
  3.0 Vdc to 16 Vdc (MC14081CL/CP)
- Single Supply Operation Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout

McMOS

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "AND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

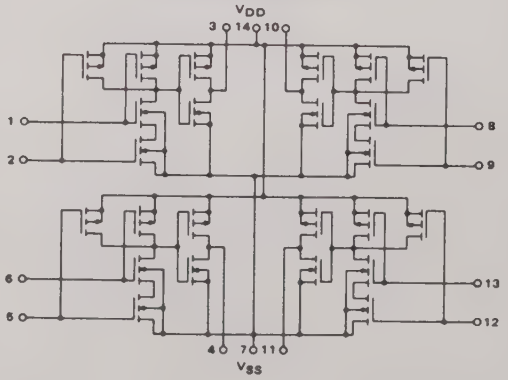
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

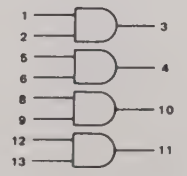
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14081AL MC14081CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	—MC14081AL —MC14081CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



LOGIC DIAGRAM



3 = 1 • 2

V_{DD} = Pin 14
V_{SS} = Pin 7

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MC14175B

McMOS SSI

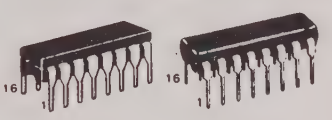
(LOW-POWER COMPLEMENTARY MOS)

QUAD TYPE D FLIP-FLOP

QUAD TYPE D FLIP-FLOP

The MC14175B quad type D flip-flop is constructed with MOS P channel and N-channel enhancement mode devices in a single monolithic structure. Each of the four flip-flops is positive-edge triggered by a common clock input (C). An active-low reset input ($\overline{R}$) asynchronously resets all flip-flops. Each flip-flop has independent Data (D) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Complementary Outputs
- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Output Compatible with Two HTL Loads, Two Low-Power TTL Loads or One Low-Power Schottky TTL Load
- Functional Equivalent to TTL 74175



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

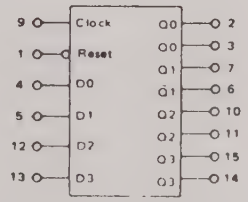
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE
(Positive Logic)

INPUTS			OUTPUTS		
Clock	Data	$\overline{Reset}$	Q	$\overline{Q}$	
↑	0	1	0	1	
↑	1	1	1	0	
↓	X	1	Q	$\overline{Q}$	No Change
X	X	0	0	1	

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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MC14419

2-OF-8 KEYPAD-TO-BINARY ENCODER

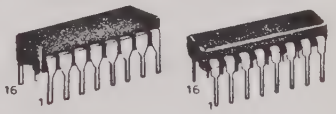
The MC14419 is designed for phone dialer system applications, but finds many applications as a keypad-to-binary encoder. The device contains a 2-of-8 to binary encoder, a strobe generator, and an illegal state detector. The encoder has four row inputs and four column inputs, and is designed to accept inputs from 16 keyswitches arranged in a 4 x 4 matrix. For an output on the four data lines, one and only one row along with one and only one column input line must be activated. All other combinations are suppressed by the illegal state detector to eliminate false data output.

The strobe generator produces a strobe pulse when any of the 10 keys corresponding to numerals 0 through 9 are depressed. The strobe output can be used to eliminate erroneous data entry due to contact bounce. For a strobe output to occur, the key row and column input lines must remain stable for 80 clock pulses after activation. When the contact bounce has settled and 80 clock pulses have occurred, the output will be a single strobe pulse equal in width to that of the clock low state. The strobe generator will output one and only one pulse each time a numerical key is depressed. After the pulse has occurred, noise and bounce due to contact break will not cause another strobe pulse. With a 16 kHz input clock frequency, the pulse occurs 5 ms after the last bounce.

- Suppressed Output for Illegal Input Codes
- On-Chip Pullup Resistors for Row and Column Inputs
- Clock Input Conditioning Circuit
- Low Current Drain in Standby Mode
  5.0 μA Typical @ 5.0 Vdc
- Subsystem Complement to the MC14408/14409 Phone Pulse Converter
- Codes for Numbers 0-9 Produce a Strobe Pulse

McMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

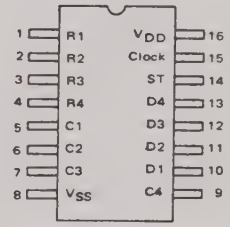
2-OF-8 KEYPAD-TO-BINARY ENCODER



L SUFFIX
CERAMIC PACKAGE
CASE 620

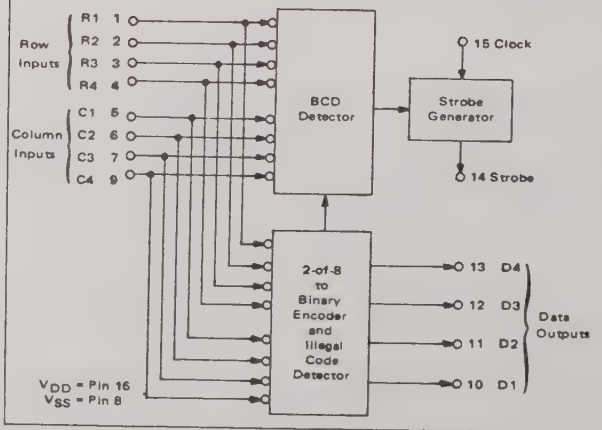
P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



V_{DD} = Pin 16
V_{SS} = Pin 8

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

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MC14503B

HEX NON-INVERTING 3-STATE BUFFER

The MC14503B is a hex non-inverting buffer with 3-state outputs, and a high current source and sink capability. The 3-state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

- 3-State Outputs
- TTL Compatible — Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Symmetrical Turn-On and Turn-off Delays
- Symmetrical Output Rise and Fall Times
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX 3-STATE BUFFER

L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXX8 — Suffix

Suffix	Denotes
L	Ceramic Package
P	Plastic Package
A	Extended Operating Temperature Range
C	Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

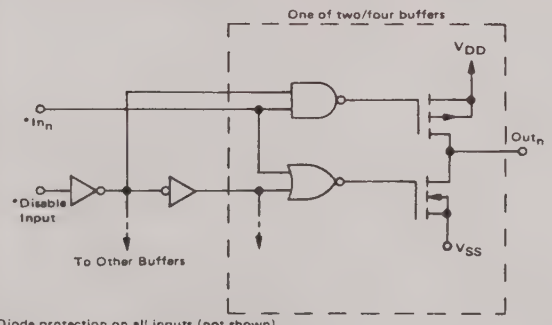
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	25	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

TRUTH TABLE

In_n	Appropriate Disable Input	Out_n
0	0	0
1	0	1
X	1	High Impedance

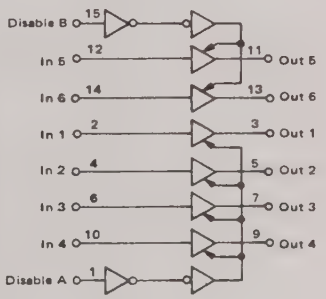
X = Don't Care

CIRCUIT DIAGRAM



*Diode protection on all inputs (not shown)

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied on an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14507AL
MC14507CL
MC14507CP

EXCLUSIVE "OR" GATE

QUAD EXCLUSIVE "OR" GATE

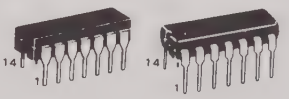
The MC14507AL/CL quad exclusive OR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 2.5 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14507AL)
  3.0 Vdc to 16 Vdc (MC14507CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-For-Pin Compatible with 4030 Type

McMOS

(LOW-POWER COMPLEMENTARY MOS)

QUAD EXCLUSIVE "OR" GATE



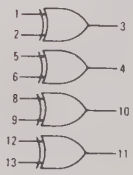
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating		Symbol	Value	Unit
DC Supply Voltage	–MC14507AL –MC14507CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	–MC14507AL –MC14507CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

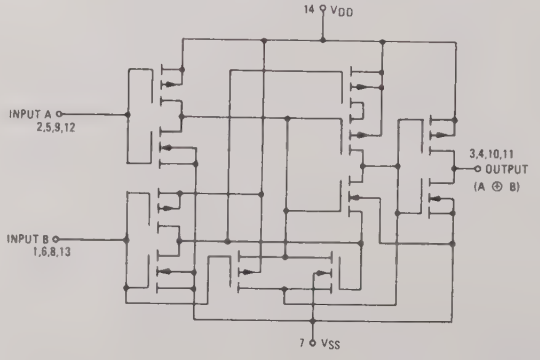
LOGIC DIAGRAM
POSITIVE LOGIC



3 = 1⊕2

V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATIC
(1/4 OF DEVICE SHOWN, BUT ALL PIN NUMBERS INDICATED)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14511AL
MC14511CL
MC14511CP

LATCH/DECODER/DRIVER

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

The MC14511 BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

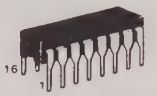
Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility

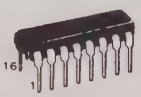
McMOS

(LOW-POWER COMPLEMENTARY MOS)

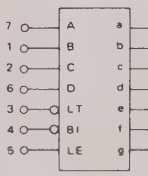
BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648



V_{DD} = Pin 16
V_{SS} = Pin 8

DISPLAY

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage – MC14511AL – MC14511CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
Operating Temperature Range – MC14511AL – MC14511CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Maximum Continuous Output Drive Current (Source) per Output	I_{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output ‡	P_{OHmax}	50	mW

‡ $P_{OHmax} = I_{OH}(V_{DD} - V_{OH})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occure if V_{in} and V_{out} is not constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

TRUTH TABLE

INPUTS							OUTPUTS							
LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X								*

X = Don't Care
*Depends upon the BCD code previously applied when LE = 0

MC14518AL
MC14518CL
MC14518CP
MC14520AL
MC14520CL
MC14520CP

DUAL UP COUNTERS

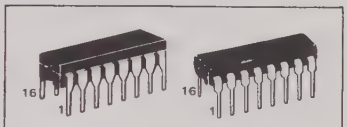
The MC14518 dual BCD counter and the MC14520 dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518 will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Quiescent Power Dissipation = 1.0 μW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14518AL and MC14520AL)
  = 3.0 Vdc to 16 Vdc (MC14518CL,CP and MC14520CL,CP)
- Low Input Capacitance = 5.0 pF typical
- Internally Synchronous for High Internal and External Speeds.
- Logic Edge-Clocked Design – Incremented on Positive Transition of Clock or Negative Transition on Enable
- 6.0 MHz Counting Rate

McMOS

(LOW-POWER COMPLEMENTARY MOS)

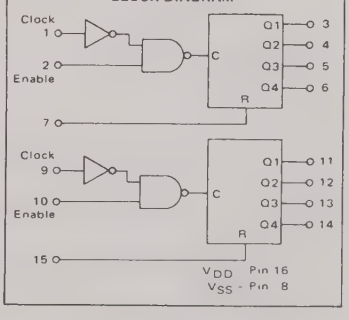
DUAL BCD UP COUNTER
(MC14518)
DUAL BINARY UP COUNTER
(MC14520)



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage –MC14518AL/520AL –MC14518CL,CP/520CL,CP	V_{DD}	+18 to –0.5 +16 to –0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to –0.5	Vdc
DC Current Drain Per Pin	I	10	mAdc
Operating Temperature Range MC14518AL/520AL MC14518CL,CP/520CL,CP	T_A	 –55 to +125 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q1 thru Q4 = 0

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

MC14519AL
MC14519CL
MC14519CP

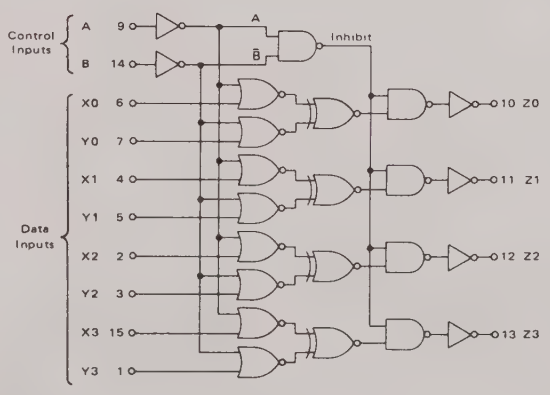
4-BIT AND/OR SELECTOR
or
QUAD 2-CHANNEL DATA SELECTOR
or
QUAD EXCLUSIVE "NOR" GATE

The MC14519 is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

This device exemplifies the design versatility of MCMOS logic structure. This part provides three functions in one package; a **4-Bit AND/OR Selector,** a **Quad 2-Channel Data Selector,** or a **Quad Exclusive NOR Gate.**

- Quiescent Power Dissipation = 25 nW/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14519AL)
  3.0 Vdc to 16 Vdc (MC14519CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Plug-In Replacement for CD4019 in Most Applications

LOGIC DIAGRAM
(Positive Logic)



V_{DD} = Pin 16
V_{SS} = Pin 8

McMOS

(LOW-POWER COMPLEMENTARY MOS)

4-BIT AND/OR SELECTOR

L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

TRUTH TABLE

CONTROL INPUTS		OUTPUT
A	B	Z_n
0	0	0
0	1	Y_n
1	0	X_n
1	1	$X_n \circledcirc Y_n$

Note:
$X_n \circledcirc Y_n$ means X_n (Exclusive-NOR) Y_n

MC14527AL
MC14527CL
MC14527CP

BCD RATE MULTIPLIER

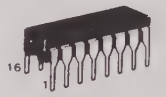
The MC14527 BCD rate multiplier (DRM) provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD input number, there will be six output pulses for every ten input pulses. This part may be used to add, subtract, divide, raise to power, and solve algebraic and differential equations, and can be used to generate trigonometric functions and natural logarithms. Typical applications include digital filters, motor speed control and frequency synthesizers.

- Quiescent Power Dissipation = 0.25 μW/package typical @ 5.0 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14527AL)
  = 3.0 Vdc to 16 Vdc (MC14527CL/CP)
- Low Input Capacitance – 5.0 pF typical
- Internally Synchronous for High Speed
- Output Clocked on the Negative Going Edge of Clock
- Strobe for Inhibiting or Enabling Outputs
- Enable and Cascade Inputs for Cascade Operation of Two or More DRMs
- "9" Output for the Parallel Enable Configuration and DRMs in Cascade
- Complementary Outputs
- Clear and Set to Nine Inputs

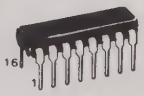
McMOS

(LOW POWER COMPLEMENTARY MOS)

BCD RATE MULTIPLIER

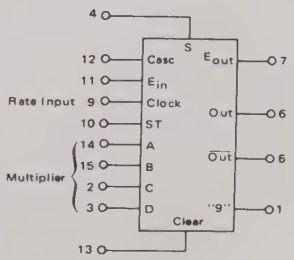


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14527AL MC14527CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14527AL – MC14527CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS										OUTPUT LOGIC LEVEL NUMBER OF PULSES			
D	C	B	A	No. of Clock Pulses	E_{in}	STROBE	CASCADE	CLEAR	SET	OUT	$\overline{OUT}$	E_{out}	"9"
0	0	0	0	10	0	0	0	0	0	0	1	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	–	–	–	–
X	X	X	X	10	0	1	0	0	0	0	1	1	1
X	X	X	X	10	0	0	1	0	0	1	0	1	1
1	X	X	X	10	0	0	0	1	0	10	10	1	0
0	X	X	X	10	0	0	0	1	0	0	1	1	0
X	X	X	X	10	0	0	0	0	1	0	1	0	1

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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MC14528B

DUAL MONOSTABLE MULTIVIBRATOR

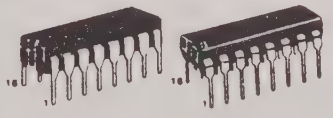
The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X.

- Separate Reset Available
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL
RETRIGGERABLE/RESETTABLE
MONOSTABLE MULTIVIBRATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

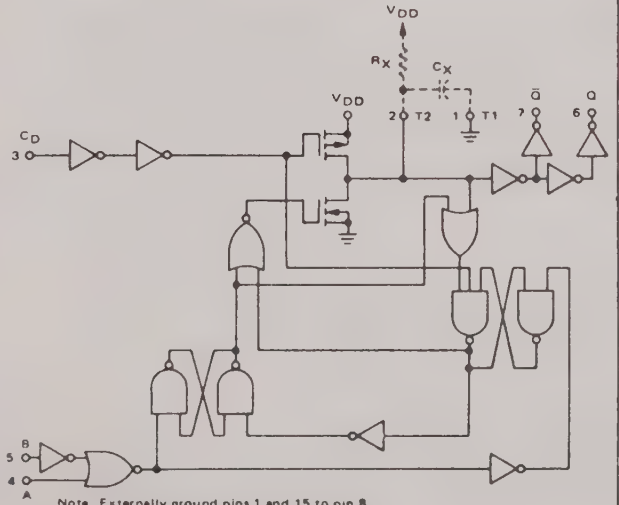
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

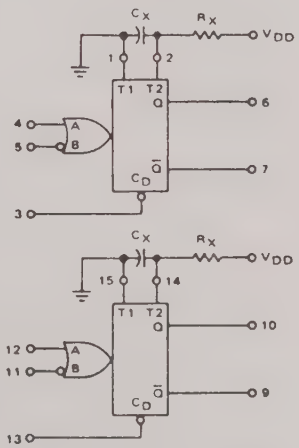
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM
(1/2 of Device Shown)



Note: Externally ground pins 1 and 15 to pin 8.

BLOCK DIAGRAM



RX and CX are external components.

VDD = Pin 16
VSS = Pin 8

MC14532AL
MC14532CL
MC14532CP

PRIORITY ENCODER

8-BIT PRIORITY ENCODER

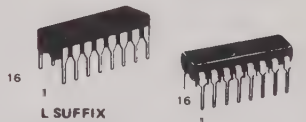
The MC14532AL/CL/CP is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input (E_{in}) are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output (E_{out}).

- Quiescent Power Dissipation = 25 nW/package typical @ 5.0 Vdc
- Noise immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Low Input Capacitance – 5.0 pF typical

McMOS

(LOW-POWER COMPLEMENTARY MOS)

8-BIT PRIORITY ENCODER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltage referenced to V_{SS}, Pin 8)

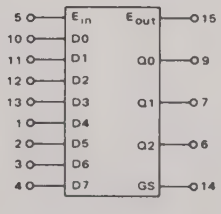
Rating	Symbol	Value	Unit
DC Supply Voltage MC14532AL MC14532CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range—MC14532AL —MC14532CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUT									OUTPUT				
E_{in}	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_{out}
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

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MC14572

HEX GATE

The MC14572 hex functional gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. The chip contains four inverters, one NOR gate and one NAND gate.

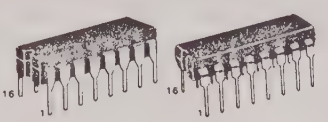
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Single Supply Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Input Impedance = 10^{12} ohms typical
- NOR Input Pin Adjacent to V_{SS} Pin to Simplify Use As An Inverter
- NAND Input Pin Adjacent to V_{DD} Pin to Simplify Use As An Inverter
- NOR Output Pin Adjacent to Inverter Input Pin For OR Application
- NAND Output Pin Adjacent to Inverter Input Pin For AND Application
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX GATE

4 INVERTERS PLUS
2-INPUT NOR GATE PLUS
2-INPUT NAND GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

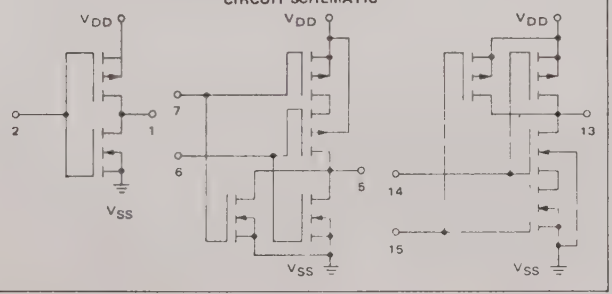
ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

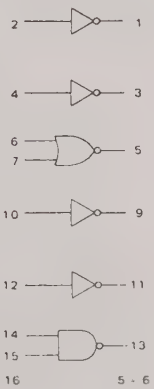
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

5 • 6 • 7
13 • 14 • 15

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MC14584B

Advance Information

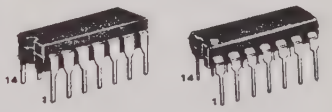
McMOS SSI
(LOW-POWER COMPLEMENTARY MOS)

HEX SCHMITT TRIGGER

HEX SCHMITT TRIGGER

The MC14584B hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14584B may be used in place of the MC14069B hex inverter for enhanced noise immunity or to "square up" slowly changing waveforms.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD40106B and MM74C14
- Can Be Used to Replace MC14069B



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

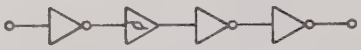
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

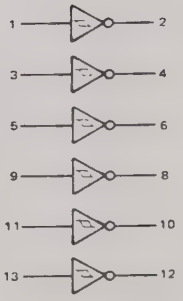
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

EQUIVALENT CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This is advance information and specification are subject to change without notice.

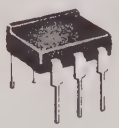
4N25
4N26
4N27
4N28

NPN PHOTOTRANSISTOR AND PN INFRARED EMITTING DIODE

. . . Gallium Arsenide LED optically coupled to a Silicon Photo Transistor designed for applications requiring electrical isolation, high-current transfer ratios, small package size and low cost; such as interfacing and coupling systems, phase and feedback controls, solid-state relays and general-purpose switching circuits.

- High Isolation Voltage — V_{ISO} = 2500 V (Min) — 4N25; 1500 V (Min) — 4N26, 4N27; 500 V (Min) — 4N28
- High Collector Output Current @ I_F = 10 mA — I_C = 5.0 mA (Typ) — 4N25, 4N26; 3.0 mA (Typ) — 4N27, 4N28
- Economical, Compact, Dual-In-Line Package
- Excellent Frequency Response — 300 kHz (Typ)
- Fast Switching Times @ I_C = 10 mA t_{on} = 0.87 μs (Typ) — 4N25, 4N26; 2.1 μs (Typ) — 4N27, 4N28; t_{off} = 11 μs (Typ) — 4N25, 4N26; 5.0 μs (Typ) — 4N27, 4N28

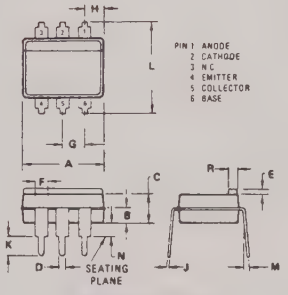
INFRARED LIGHT EMITTING DIODE PHOTOTRANSISTOR COUPLED PAIR



*MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE MAXIMUM RATINGS			
Reverse Voltage	V_R	3.0	Volts
Forward Current — Continuous	I_F	80	mA
Forward Current — Peak (Pulse Width = 300 μs, 2.0% Duty Cycle)	I_F	3.0	Amp
Total Device Dissipation @ T_A = 25°C Negligible Power in Transistor Derate above 25°C	P_D	150 2.0	mW mW/°C
PHOTOTRANSISTOR MAXIMUM RATINGS			
Collector-Emitter Voltage	V_{CEO}	30	Volts
Emitter-Collector Voltage	V_{ECO}	7.0	Volts
Collector-Base Voltage	V_{CBO}	70	Volts
Total Device Dissipation @ T_A = 25°C Negligible Power in Diode Derate above 25°C	P_D	150 2.0	mW mW/°C
TOTAL DEVICE RATINGS			
Total Device Dissipation @ T_A = 25°C Equal Power Dissipation in Each Element Derate above 25°C	P_D	250 3.3	mW mW/°C
Junction Temperature Range	T_J	-55 to +100	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Soldering Temperature (10 s)		260	°C

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.38	8.89	0.330	0.350
B	1.40	1.65	0.055	0.065
C	2.92	3.18	0.115	0.125
D	0.41	0.51	0.016	0.020
E	0.84	0.89	0.025	0.035
F	1.14	1.40	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	1.57	1.83	0.062	0.072
J	0.23	0.28	0.009	0.011
K	2.54	3.30	0.100	0.130
L	7.37	7.87	0.290	0.310
M	–	90°	–	90°
N	–	1.27	–	0.050
R	1.52	1.78	0.060	0.070

CASE 673-03

FIGURE 1 — MAXIMUM POWER DISSIPATION

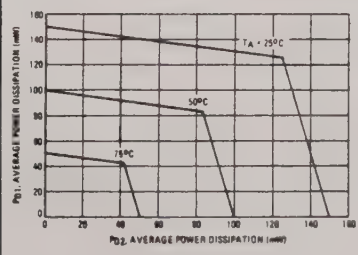


Figure 1 is based upon using limit values in the equation

$T_{J1} - T_A = R_{\theta JA}(P_{D1} + K_\theta P_{D2})$

where

T_{J1} Junction Temperature (100°C)

T_A Ambient Temperature

$R_{\theta JA}$ Junction to Ambient Thermal Resistance (500°C/W)

P_{D1} Power Dissipation in One Chip

P_{D2} Power Dissipation in Other Chip

K_θ Thermal Coupling Coefficient (20%)

Example:

With P_{D1} = 90 mW in the LED @ T_A = 50°C, the transistor P_D (P_{D2}) must be less than 50 mW

4096 Bit High Speed Electrically Alterable Read Only Memories

FEATURES

- 1024 × 4 Organization, Fully Decoded
- Single Word or Block Electrically Erasable
- TTL Compatible with Resistor Pull-ups
- Three State Output
- ER3400: 650ns Access Time
- ER3401: 950ns Access Time
- 1.8 us Cycle Time
- 10 ms Word or Block Erase Time
- 1 ms Write Time
- 22 Pin DIP
- P-Channel Metal Gate MNOS Technology
- 0°C to 70°C Operation
- +5, -12, -30V Power Supplies
- 10^5 Erase-Write Cycles per Word
- 2×10^{11} Read Cycles per Word
- 10 Year Unpowered Nonvolatile Data Storage — 10 Years

DESCRIPTION

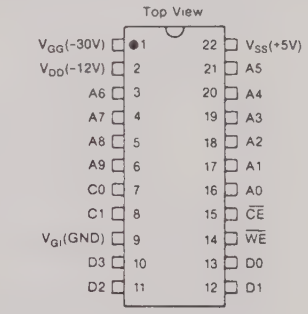
The ER3400 and ER3401 are word alterable ROMs intended for use as read-mostly memories. Each operates with one clock, CHIP ENABLE ($\overline{CE}$), which also serves for chip selection. All other pins of each device can be paralleled with other EAROMs.

Any one of four possible operating modes can be selected by setting the proper binary code on the C0-C1 control lines and pulsing the device with $\overline{CE}$. The four modes are Read, Write, Word Erase and Block Erase. The ER3400/3401 will sense the control lines and change modes only when pulsed by $\overline{CE}$. When in the Read mode, data is read during each $\overline{CE}$ pulse. Writing or erasing of a word continues for as long as the device is in the Write or Erase mode. Each write or erase word cycle must be ended by a dummy read operation.

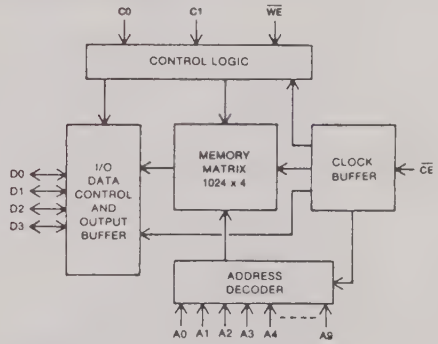
A WRITE ENABLE ($\overline{WE}$) input pulse indicates to the ER3400/3401 that the data on the D_0-D_3 data input/output lines is valid input data. This data is then stored internally for use during the write operation.

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



No particular order of power supply sequencing on or off i required for the ER3400. Circuits are provided to force the devic into the read mode during power turn on. Erasing and writing ar inhibited if V_{DD} or V_{GG} are not at proper operating levels.

For the ER3401, V_{GG} must be turned on after V_{DD} is stable an removed before V_{DD} is turned off.

PIN FUNCTIONS

A_0-A_9	10-Bit Word Address
D_0-D_3	Data input and output pins
$\overline{CE}$	Chip Enable. Chip selected when $\overline{CE}$ is pulsed to logic "0".
C_0, C_1	Mode Control Inputs
	C0 C1 0 1 Block Erase Mode: erase operation performed on all words. 1 1 Word Erase Mode: stored data is erased at addressed location. 0 0 Read Mode: addressed data read after leading edge of $\overline{CE}$ pulse. 1 0 Write Mode: input data written at addressed location.
$\overline{WE}$	Write Enable. Input data read when $\overline{WE}$ is pulsed to logic "0".
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input
V_{DD}	Power Supply Input. Normally at -12 volts.
V_{GG}	Power Supply Input. Normally at -30 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (with respect to V_{SS}) ..... -40V to +0.3V
Storage temperature (with data retention) ..... -40°C to +70°C
Storage temperature (without data retention) ..... -65°C to +150°C
Soldering temperature of leads (10 seconds) .....+300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = +5V ±5%
V_{DD} = -12V ±5%
V_{GG} = -30V ±5%
V_{GI} = GND
Operating Temperature (T_A) = 0°C to =70°C

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input Logic "1"	V_{IH}	V_{SS}-1.5	—	V_{SS}+0.3	Volts	
Input Logic "0"	V_{IL}	-10	—	0.8	Volts	
Output Logic "1"	V_{OH}	V_{SS}-1.5	—	—	Volts	I_{OH} = -2mA
Output Logic "0"	V_{OL}	—	—	0.4	Volts	I_{OL} = 2mA
Control Input Leakage	I_{LC}	—	—	-2.0	μA	V_{IN} = V_{SS} -15 Volts
Data Input Leakage	I_{LD}	—	—	-10.0	μA	V_{IN} = V_{SS} -15 Volts
Power Supply Current						
V_{DD} Supply Current: Chip selected	I_{DD}	—	—	-25.0	mA	V_{DD} = V_{SS} -17 Volts
Chip de-selected	I_{DD}	—	—	-7.0	mA	V_{DD} = V_{SS} -17 Volts
V_{GG} Supply Current	I_{GG}	—	—	-3.0	mA	V_{GG} = V_{SS} -35 Volts
V_{SS} Supply Current: Chip selected	I_{SS}	—	—	-29.0	mA	V_{DD} = V_{SS} -17V, V_{GG} = V_{SS} -35V
Chip de-selected	I_{SS}	—	—	-11.5	mA	V_{DD} = V_{SS} -17V, V_{GG} = V_{SS} -35V
AC CHARACTERISTICS						
Input capacitance - control inputs	C_I	—	6	8	pf	
Input capacitance - data inputs	C_D	—	8	10	pf	
Read Mode Characteristics						
Address and control to $\overline{CE}$	t_{D1}	0	—	—	ns	
Address and control hold time	t_{D2}	250	—	—	ns	
$\overline{CE}$ to Data I/O Off	t_{D3}	50	—	200	ns	
$\overline{CE}$ high	t_{D4}	900	—	—	ns	
Access time: ER3400	t_A	—	—	650	ns	RL = 2K to V_{SS}, CL = 100pf
ER3401	t_A	—	—	950	ns	RL = 2K to V_{SS}, CL = 100pf
$\overline{CE}$ pulse width: ER3400	$t_{\overline{CE}}$	650	—	100000	ns	
ER3401	$t_{\overline{CE}}$	950	—	100000	ns	
Read cycle time	t_{CY}	$1650+t_r+t_f$	—	—	—	
$\overline{CE}$ rise, fall time	t_r, t_f	0	—	100	ns	
Write/Erase Mode Characteristics						
Address and control to $\overline{CE}$	t_{D11}	0	—	—	ns	
Address and control hold time	t_{D12}	250	—	—	ns	
$\overline{CE}$ fall to $\overline{WE}$ fall delay	t_{D13}	0	—	—	ns	$\overline{WE}$ rise may overlap $\overline{CE}$ rise by a maximum of 50ns.
$\overline{WE}$ rise to $\overline{CE}$ rise delay	t_{D14}	-50	—	—	ns	$\overline{WE}$ rise may overlap $\overline{CE}$ rise by a maximum of 50ns.
Data stable to $\overline{WE}$	t_{D15}	0	—	—	ns	$\overline{WE}$ rise may overlap $\overline{CE}$ rise by a maximum of 50ns.
$\overline{WE}$ rise to End of Data Stable	t_{D16}	50	—	—	ns	$\overline{WE}$ rise may overlap $\overline{CE}$ rise by a maximum of 50ns.
$\overline{CE}$ pulse width: ER3400	$t_{\overline{CE}}$	650	—	100000	ns	
ER3401	$t_{\overline{CE}}$	950	—	100000	ns	
WE pulse width	$t_{\overline{WE}}$	400	—	—	ns	
Write time	t_W	1	—	2	ms	
Erase time	t_E	10	—	20	ms	

**Typical values are at +25°C and nominal voltages.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

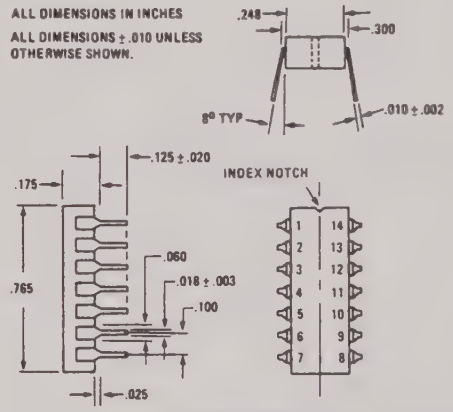
HM1-0110 (4x10)
HM1-0168 (6x 8)
HM1-0104 (10x 4)
HM1-0186 (8x 6)
Commercial Diode Matrix

DESCRIPTION

The commercial diode matrices are arrays of passivated silicon diodes, fabricated in dielectrically isolated moats. An epitaxial layer is used as the common cathode connection for all diodes in a row. Column connections to the anode side of the diodes are made through metal interconnect lines via fusible links. By selectively opening the links, diodes can be removed from the circuit to form any desired matrix pattern. This device is available in a 14-lead dual in-line CERDIP package.

PACKAGE

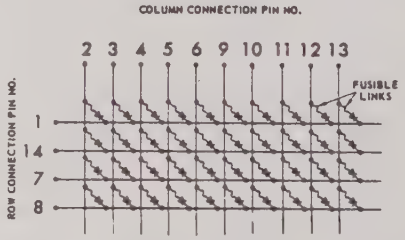
CODE 1A



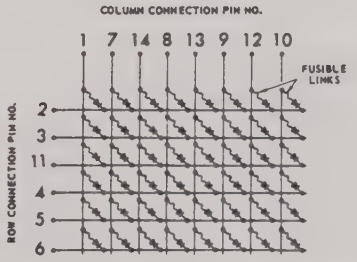
14 LEAD CERDIP

MATRIX PATTERNS

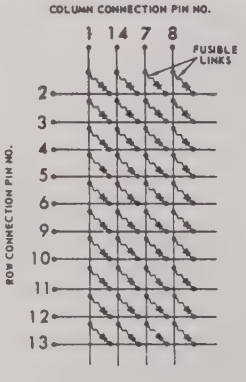
HM1-0110 - 5
(4 x 10)



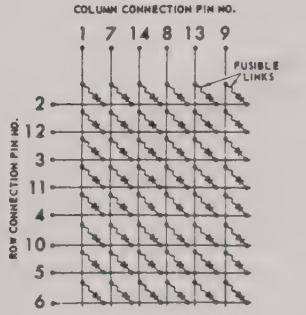
HM1-0168 - 5
(6 x 8)



HM1-0104
(10 x 4)



HM1-0186
(8 x 6)



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ABSOLUTE MAXIMUM RATINGS

Forward Current	100mA
Surge Current (100 µs Max.)	200mA
Total Circuit Dissipation (Still Air)	450mW
Operating Temperature (Ambient)	0°C to 70°C

ELECTRICAL CHARACTERISTICS AT 25°C

CHARACTERISTIC		HM1-0104 (10 x 4) HM1-0168 (6 x 8) HM1-0186 (8 x 6) LIMITS		HM1-0110 (4 x 10) LIMITS		CONDITIONS
		MIN.	MAX.	MIN.	MAX.	
Forward Drop	V_{F20}		1.5V		1.8V	I_F = 20mA
Forward Drop	V_{F1}		0.9V		1.0V	I_F = 1mA
Rev. Breakdown Volt.	BV_R	20V		20V		I_R = 100µA
Rev. Current	I_R		1µA		1µA	V_R = 15V
Rev. Rec. Time			100ns		100ns	I_F = 10mA I_R = 10mA to 1mA
Coupling Capacitance	C_{CP}		8pF		8pF	V_R = 5V f = 1MHz

NOTE: When ordering a matrix with a custom pattern either obtain copies of Harris patternizing forms from your local sales representative or contact headquarters, Marketing, Melbourne, Florida.

On all orders less than 100 units there will be a one time charge for each special pattern formed by Harris.

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Consumer Circuits

LM380 audio power amplifier general description

The LM380 is a power audio amplifier for consumer application. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows inputs to be ground referenced. The output is automatically self entering to one half the supply voltage.

The output is short circuit proof with internal thermal limiting. The package outline is standard dual-in-line. A copper lead frame is used with the center three pins on either side comprising a heat sink. This makes the device easy to use in standard p-c layout. A mini dual-in-line package version with reduced power capability also available.

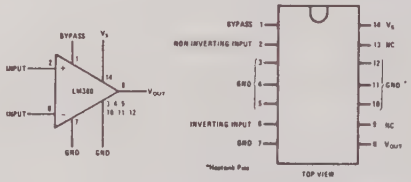
Uses include simple phonograph amplifiers, intercoms, line drivers, teaching machine outputs, alarms, ultrasonic drivers, TV sound systems, AM-FM radio, small servo drivers, power converters,etc.

features

- Wide supply voltage range
- Low quiescent power drain
- Voltage gain fixed at 50
- High peak current capability
- Input referenced to GND
- High input impedance
- Low distortion
- Quiescent output voltage is at one-half of the supply voltage
- Standard dual-in-line package

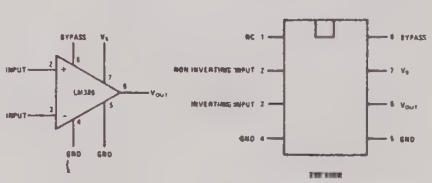
block and connection diagrams

Dual-In-Line Package



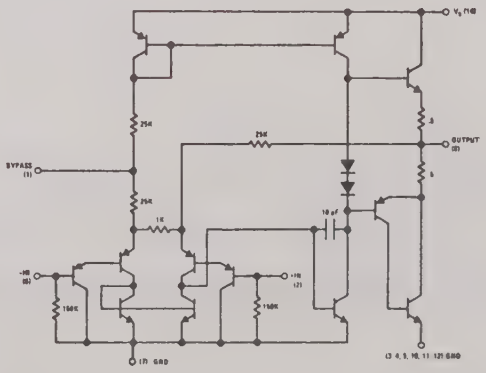
Order Number LM380N
See Package 22

Dual-In-Line Package



Order Number LM380N-8
See Package 20

schematic diagram



DESCRIPTION

The NE/SE 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA or drive TTL circuits.

FEATURES

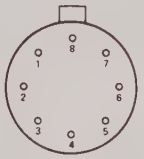
- TIMING FROM MICROSECONDS THROUGH HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- ADJUSTABLE DUTY CYCLE
- HIGH CURRENT OUTPUT CAN SOURCE OR SINK 200mA
- OUTPUT CAN DRIVE TTL
- TEMPERATURE STABILITY OF 0.005% PER °C
- NORMALLY ON AND NORMALLY OFF OUTPUT

APPLICATIONS

PRECISION TIMING
PULSE GENERATION
SEQUENTIAL TIMING
TIME DELAY GENERATION
PULSE WIDTH MODULATION
PULSE POSITION MODULATION
MISSING PULSE DETECTOR

PIN CONFIGURATIONS

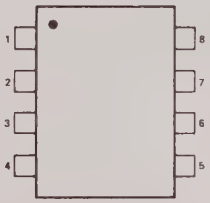
T PACKAGE
(Top View)



1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

ORDER PART NOS. SE555T/NE555T

V PACKAGE
(Top View)



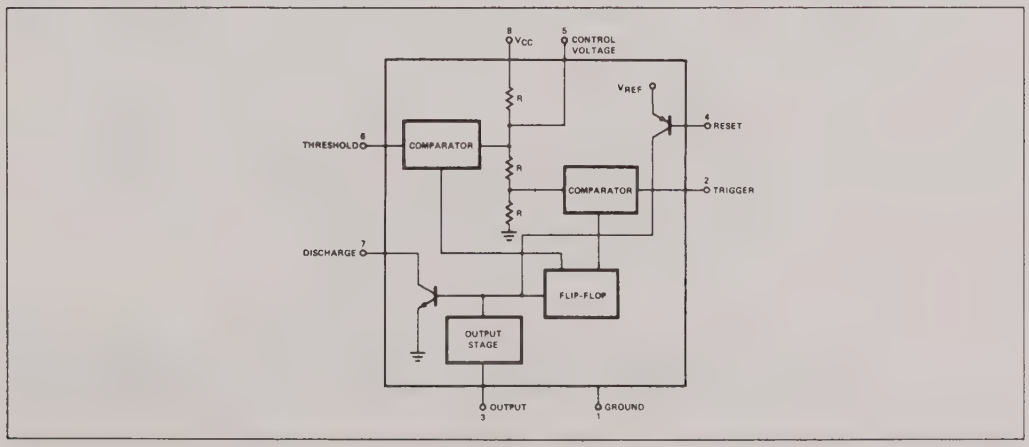
1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

ORDER PART NOS. SE555V/NE555V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18V
Power Dissipation	600 mW
Operating Temperature Range	
NE555	0°C to +70°C
SE555	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

BLOCK DIAGRAM



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DESCRIPTION

The NE/SE556 Dual Monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 150mA.

FEATURES

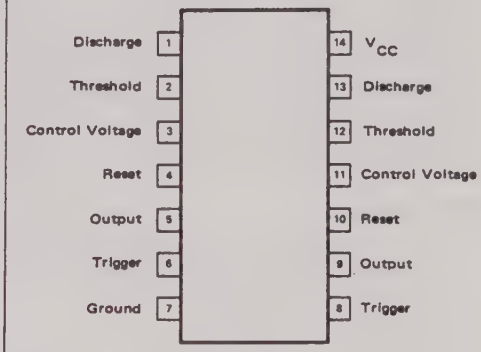
- TIMING FROM MICROSECONDS TO HOURS
- REPLACES TWO 555 TIMERS
- OPERATES IN BOTH ASTABLE, MONOSTABLE, TIME DELAY MODES
- HIGH OUTPUT CURRENT
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.05% PER °C

APPLICATIONS

PRECISION TIMING
SEQUENTIAL TIMING
PULSE SHAPING
PULSE GENERATOR
MISSING PULSE DETECTOR
TONE BURST GENERATOR
PULSE WIDTH MODULATION
TIME DELAY GENERATOR
FREQUENCY DIVISION
INDUSTRIAL CONTROLS
PULSE POSITION MODULATION
APPLIANCE TIMING
TRAFFIC LIGHT CONTROL
TOUCH TONE ENCODER

PIN CONFIGURATION (Top View)

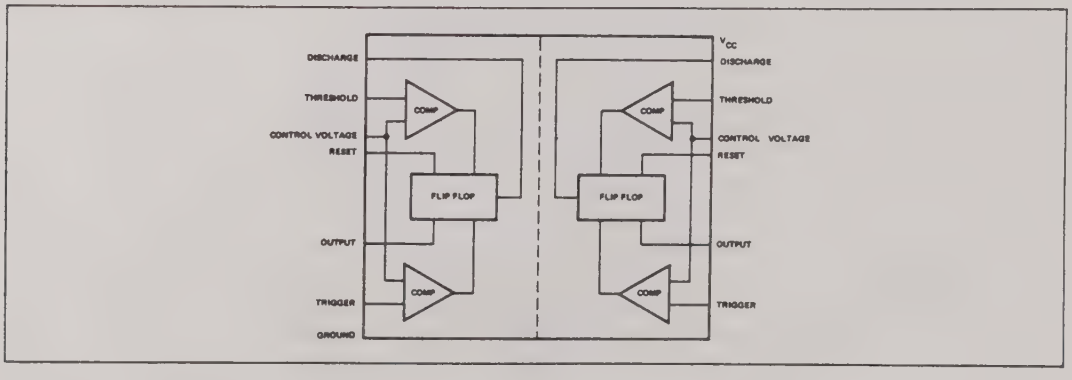
A PACKAGE



ABSOLUTE MAXIMUM RATINGS

Supply Voltage		+18V
Power Dissipation		600mW
Operating Temperature Range	NE556	0°C to +70°C
	SE556	-55°C to +125°C
	SE556C	-55°C to +125°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 60 sec)		+300°C

BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +5V$ to $+15$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE 556			NE 556			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	$V_{CC} = 5V$ $R_L = \infty$		3	5		3	6	mA
	$V_{CC} = 15V$ $R_L = \infty$ Low State, Note 1		10	11		10	14	mA
Timing Error (Monostable)	$R_A = 2K\Omega$ to $100K\Omega$							
Initial Accuracy	$C = 0.1\mu F$ Note 2		0.5	1.5		0.75		%
Drift with Temperature			30	100		50		ppm/°C
Drift with Supply Voltage			0.05	0.2		0.1		%/Volt
Timing Error (Astable)	$R_A, R_B = 2K\Omega$ to $100K\Omega$							
Initial Accuracy	$C = 0.1\mu F$ Note 2		1.5			2.25		%
Drift with Temperature			90			150		ppm/°C
Drift with Supply Voltage			0.15			0.3		%/Volt
Threshold Voltage			2/3			2/3		X V_{CC}
Threshold Current	Note 3		30	100		30	100	nA
Trigger Voltage	$V_{CC} = 15V$	4.8	5	5.2		5		V
	$V_{CC} = 5V$	1.45	1.67	1.9		1.67		V
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Control Voltage Level	$V_{CC} = 15V$	9.6	10	10.4	9.0	10	11	V
	$V_{CC} = 5V$	2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage Drip (low)	$V_{CC} = 15V$							
	$I_{SINK} = 10mA$		0.1	0.15		0.1	.25	V
	$I_{SINK} = 50mA$		0.4	0.5		0.4	.75	V
	$I_{SINK} = 100mA$		2.0	2.25		2.0	2.75	V
	$I_{SINK} = 200mA$		2.5			2.5		
	$V_{CC} = 5V$							
	$I_{SINK} = 8mA$		0.1	0.25				V
	$I_{SINK} = 5mA$					.25	.35	
Output Voltage Drop (high)								
	$I_{SOURCE} = 200mA$ $V_{CC} = 15V$		12.5			12.5		
	$I_{SOURCE} = 100mA$ $V_{CC} = 15V$	13.0	13.3		12.75	13.3		V
	$V_{CC} = 5V$	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		nsec
Fall Time of Output			100			100		nsec
Discharge Leakage Current			20	100		20	100	nA
Matching Characteristics (Note 4)								
Initial Timing Accuracy			0.05	0.1		0.1	0.2	%
Timing Drift with Temperature			±10			±10		ppm/°C
Drift with Supply Voltage			0.1	0.2		0.2	0.5	%/Volt

NOTES
1. Supply current when output is high is typically 1.0ma less.
2. Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.
3. This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total R = 20 meg-ohms.
4. Matching characteristics refer to the difference between performance characteristics of each timer section.

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NOTES

APPENDIX D

LINE LEVEL PROTECTION CIRCUITS
MODELS: NLN1466A AND NLN1483A

FCC REG.: AZ489F-62518-PC-E

RINGER EQUIVALENCE: 0.5B

1. DESCRIPTION

All terminal equipment connected to telephone company lines must be registered under Part 68 of the FCC Rules and Regulations (see Appendix A), or connected through registered protective circuitry such as the NLN1466A or NLN1483A Line Level Protection Circuit described in this publication. These protective interface devices isolate the telephone network from possible damage due to customer provided equipment.

The NLN1466A Model is specifically compatible with the "Modax" 100 Radio Paging terminal and is designed for mounting inside the terminal housing. It consists of the following items:

- NLN5114A Circuit Board Assembly
- NKN6254A Telephone Plug Cable (14 FT)
- NKN6256A Interface Cable
- NLN4223A FCC Serial Plate (2 Req'd)

The NLN1483A Model is compatible with all Motorola paging terminals capable of handling line level inputs. It includes a separate housing for external mounting, and consists of the following items:

- NLN5114A Circuit Board Assembly
- NHN6308A Housing Kit
- NKN6254A Telephone Plug Cable (14 FT)
- NKN6257A Interface Cable (8 FT)
- NLN4223A FCC Serial Plate (2 Req'd)

NOTE

The NLN4309A Rack-Mount Panel Kit is available for mounting up to six NLN1483A kits in a standard 19-inch rack.

The NKN6254A Cable included with both models is terminated with a modular plug for making metallic connections to the Tip and Ring on the telephone network. The NKN6256A and NKN6257A Cables provide the interface connections between the terminal input board and the line level protection circuit.

The circuit detects ringing on the telephone line and provides a closure to the paging terminal (RU1 and RU2). The input circuit in the terminal then provides a service request closure back to the protective circuit (OH1 and OH2). This closure energizes a relay which seizes the line, and after a two-second minimum billing delay, a second relay is energized to provide the two-way audio path (CT and CR).

2. INSTALLATION

The NLN1466A Model is a factory installed option supplied with the "Modax" 100 Terminal, when either line-level input option is ordered (RO76AA/RO77AA). The information in this paragraph applies to the field installation of the NLN1483A Model.

a. Telephone Line (Metallic Connection)

Connect the modular plug (USOC RJ11C) to the receptacle (USOC RJ11W) supplied by the telephone company.

b. Terminal Connections

Refer to Table 1 and proceed as follows:

(1) Ring Detect Closure (RU1 and RU2)

When ringing is detected, a closure occurs between pins 1 and 3 of P9. Connect the BRN and ORG wires to the appropriate input pins on the terminal.

(2) Service Request Closure (OH1 and OH2)

A closure from the terminal is provided between pins 5 and 8 of P9, or pin 8 is pulled to ground, when the terminal is ready to receive data. When the closure occurs, the line will be seized and the billing delay will be started. Connect the GRN and GRY wires to the appropriate pins on the terminal input.

(3) Two-Way Audio Path (CT and CR)

After the two-second billing delay, the two-way audio path is established through pins 6 and 9 of P9. Connect the BLU and WHT wires to the appropriate pins on the terminal (BLU to Tip and WHT to Ring).

TABLE 1. INTERFACE CABLE CONNECTIONS

SIGNAL		WIRE	DESCRIPTION
NAME	PIN ON P9	COLOR	
RU1 RU2	3 1	ORG BRN	Contact closure to terminal when ringing is detected.
OH1 OH2	8 5	GRY GRN	Contact closure to protective circuit when service is requested, or pin 8 is pulled low with pin 5 at ground.
CT CR	6 9	BLU WHT	Two-way audio path. Tip and Ring respectively.
B+ Gnd	7 4	VIO YEL	DC voltage to the protective circuit. (+12 Vdc)
Key	2	----	Key-way. Live with B+.
-	10	BLK	Chassis ground.

(4) Power

DC power is applied via pins 7 and 4 of P9. Connect the VIO wire to B+ (+12 Vdc) and the YEL wire (GND) to the negative side of the power supply.

(5) Connect the BLK wire to the terminal chassis ground.

c. Rack Mounting

The NLN4309A Rack Mount Panel Kit accommodates up to six NLN1483A Line Level Protection Circuits. It includes the hardware required for attaching the housings to the panel and the panel to the rack. Proceed as follows:

(1) Determine the desired rack location for the panel and secure it to the rack using the following hardware items (four of each):

Part No.	Description
0205483A01	Nut, clip-on
0305925A01	Screw, machine, pan head, phillips
0400002647	Lockwasher, #10
0400135784	Washer, flat

NOTE

Due to space limitations at some sites, it may be easier to attach the protective circuit kits to the panel before installing the panel in the rack.

(2) Attach the protective circuit kit(s) to the panel using two of the following hardware items for each kit:

Part No.	Description
0300136993	Screw, machine, #6-32 x 3/8"
0400007666	Lockwasher, #6

(3) Secure the cables using the two adhesive backed clamps (Part No. 4205565D01) and six tie straps (Part No. 4210217A02) supplied.

3. OPERATION (Refer to the Schematic Diagram)

The ring detector portion of the circuit is always connected across the tip and ring on the telephone line. Capacitor C1 provides dc isolation and couples the ringing frequency to the ring detect circuit. The primary of transformer T1 is not connected across the line due to open contacts of relay K1.

When ringing occurs on the line, the tone is rectified by the diode bridge. The resulting dc level causes the diode in optical coupler U1 to emit light. This causes the transistor in U1 to appear forward biased and produce current through resistor R2. This output is integrated by C2 and C3. After several cycles of ringing current, capacitor C3 becomes sufficiently charged to turn on Q1 and thereby energize relay K2.

When K2 is energized, contacts close across pins 3 and 1 on P9 (RU1 and RU2 respectively). This signals the terminal that a caller has rung the terminal. When the terminal has processed the ring signal and is ready to receive the call, the terminal supplies a contact closure (or a saturated transistor) across pins 8 and 5 on P9 (OH1 and OH2 respectively). This presents a ground at pin 8 which energizes relay K1 and also turns off transistor Q2. When K1 is energized, contacts close and connect the telephone line to the primary of transformer T1. This seizes the line. However, the secondary of T1 is open at this time due to the open contacts of relay K3.

When Q3 is turned off by the signal at pin 8 of P9, capacitor C5 begins charging through R7 and R8. The charge time is selected to be about 2.5 seconds, guaranteeing a minimum billing delay of 2 seconds. When C5 charges sufficiently, Q3 turns on, which energizes relay K3. This closes the circuit path from T1 to pin 6 on P9. A two-way audio path now exists from the telephone line to the terminal input, with isolation provided by T1.

The collector voltage for Q2 is regulated by VR3 to provide a consistent reference voltage for the timing circuit. This permits the unregulated dc supply from the terminal to vary slightly without appreciably changing the billing delay time.

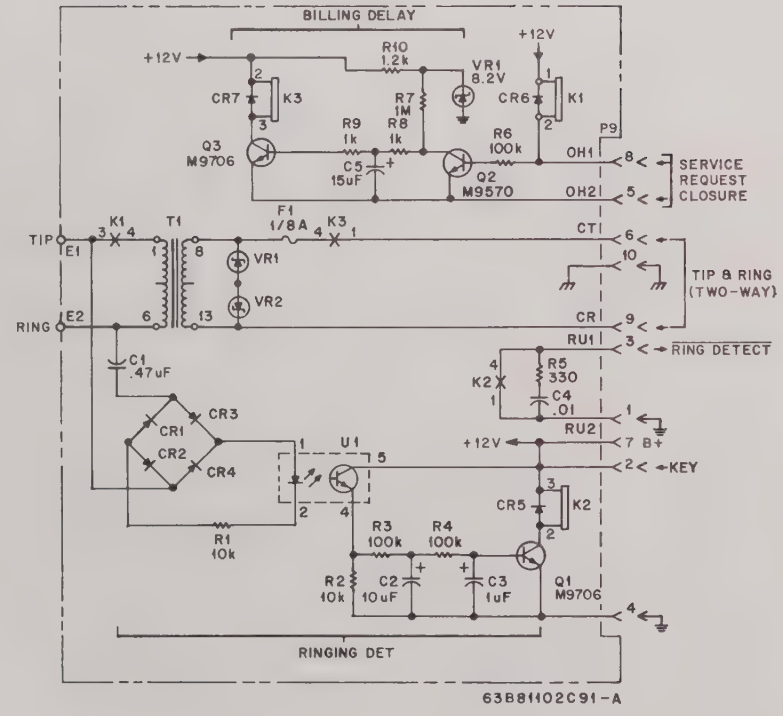
4. MAINTENANCE

Refer to the schematic diagram, circuit board detail, and parts list for maintenance information.

CAUTION

This registered equipment may only be serviced by authorized Motorola Service Station personnel. Return to the nearest Motorola Service Station for maintenance.

SCHEMATIC DIAGRAM

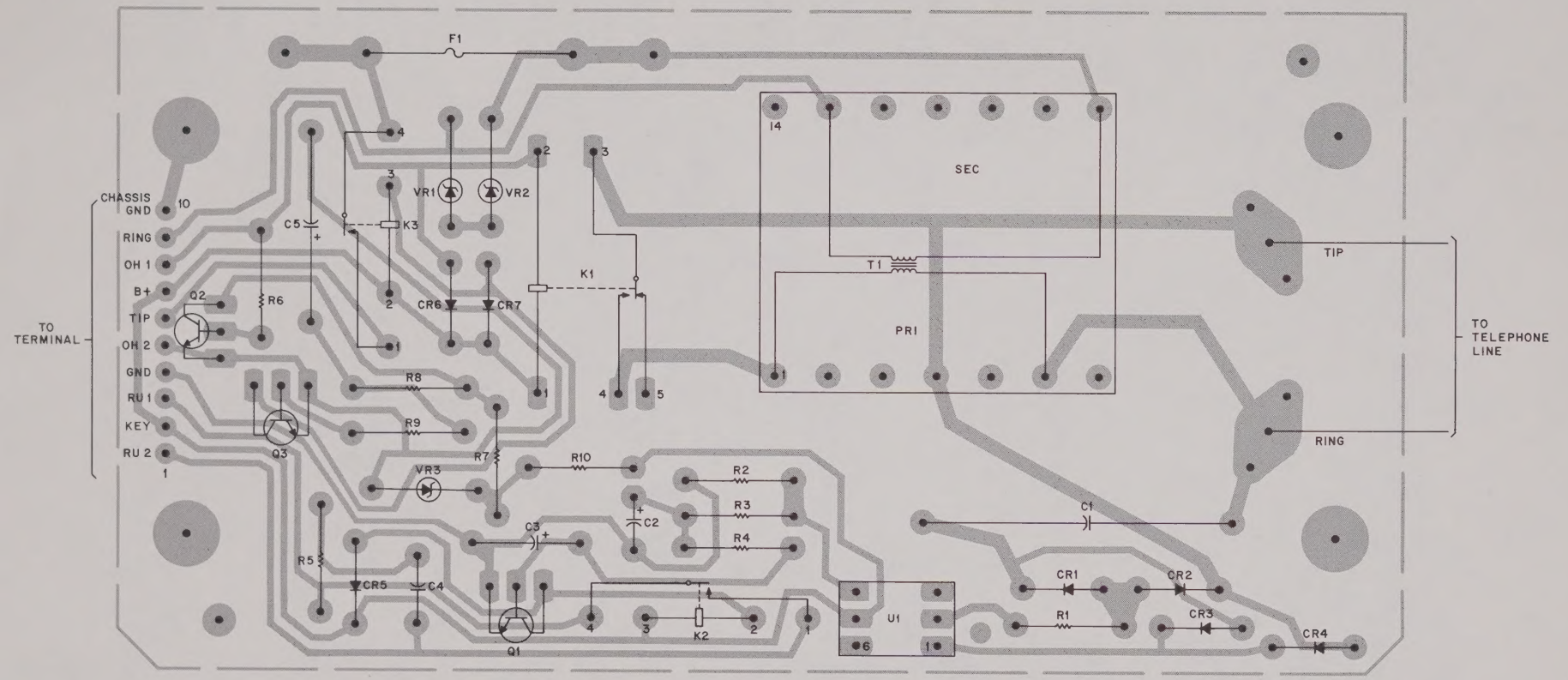


NLN5144A Line Level Protective Circuit PLF-1435-O

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		CAPACITOR; Fixed: uF ±20%; 20 V unless stated
C1	0800863994	0.47 ±10%; 200 V
C2	2383441B19	10
C3	2384762H06	1, 35 V
C4	2182428B12	0.01 +10 -30%, 100 V
C5	2383214C16	15 ±5%
		DIODE: See Note
CR1-4	4882466H18	Silicon; PIV 700 V
CR5-7	4882466H01	Silicon
		TERMINAL:
E1, 2	2983462G01	Screw
		FUSE:
F1	6500139681	3 AG, 1/8 A
		CONNECTOR:
J1	0905261D02	Male, 10-pin
		RELAY:
K1	8005170G01	1 Form C
K2, 3	8005103G01	1 Form A
		TRANSISTOR: See Note
Q1	4800869706	NPN; Type M9706
Q2	4800869570	NPN; Type M9570
Q3	4888069706	NPN; Type M9706
		RESISTOR, Fixed: Ω ±5%; 1/4 W
R1, 2	0600124A73	10 k
R3, 4	0600124A97	100 k
R5	0600124A37	330 k
R6	0600124A97	100 k
R7	0600124B22	1 Megohm
R8, 9	0600124A49	1 k
R10	0600124A51	1.2 k
		TRANSFORMER:
T1	2505102G01	Isolation, 600 ohm
		INTEGRATED CIRCUIT:
U1	5184621K34	Optical Isolator, Type 4N27
		DIODE: See Note
VR1, 2	4882256C03	Zener, 4.7 V
VR3	4882256C08	Zener, 8.2 V
NONREFERENCED ITEMS		
	4210122A12	FUSEHOLDER
	8405180G01	CIRCUIT BOARD

NOTE: FCC certification requires the use of exact replacement parts. Order by Motorola part number only.

COMPONENT LOCATION DETAIL



CS DEPF-8750-0
OL DEPF-8751-0

INFORMATION SUPPLIED TO THE CUSTOMER REGARDING CONNECTION

The Commission requires that the customer be notified of the legal circumstances of connection. This is done by means of directly quoting portions of Part 68 of the F. C. C. Rules, so that the manufacturer assumes no responsibility for interpretation.

QUOTE OF APPLICABLE PORTION OF PART 68 OF THE F.C.C. RULES

"Section 68.106 Notification to Telephone Company

Customers connecting terminal equipment to the telephone network shall, before such connection is made, give notice to the telephone company of the particular line(s) to which such connection is to be made and shall provide to the telephone company the F. C. C. Registration number and the Ringer Equivalence Number of the registered terminal equipment or registered protective circuitry.

Section 68.108 Incidence of Harm

Should terminal equipment cause harm to the telephone network, the telephone company shall, where practicable, notify the customer that temporary discontinuance of service may be required; however, where prior notice is not practicable, the telephone company may temporarily discontinue service forthwith, if such action is reasonable in the circumstances. In case of such temporary discontinuance, the telephone company shall (1) promptly notify the customer of such temporary discontinuance, (2) afford the customer the opportunity to correct the situation which gave rise to the temporary discontinuance, and (3) inform the customer of his right to bring a complaint to the Commission pursuant to the procedures set out in Subpart E of this Part.

Section 68.110 Compatibility of the Telephone Network and Terminal Equipment

(b) Changes in Telephone Company Facilities, Equipment, Operations or Procedures

The telephone company may make changes in its communications facilities, equipment, operations or procedures, where such action is reasonably required in the operation of its business and is not inconsistent with the rules and regulations in this Part. If such changes can be reasonably expected to render any customer's terminal equipment incompatible with telephone company communications facilities, or require modification or alteration of such terminal equipment, or otherwise materially affect its use or performance, the customer shall be given adequate notice in writing, to allow the customer an opportunity to maintain uninterrupted service.

Section 68.218 Responsibility of Grantee of Equipment Registration

(a) In applying for a grant of an equipment registration, the grantee warrants that each unit of equipment marketed under such grant will comply with all the applicable rules and regulations in Subpart D of this Part.

(b) The grantee or its agent shall provide to the user of the registered equipment the following:

(1) Instructions concerning installation, operational and repair procedures, where applicable.

(2) Instructions that registered terminal equipment or protective circuitry may not be used with party lines or coin lines.

(3) Instructions that when trouble is experienced the customer shall disconnect the registered equipment from the telephone line to determine if the registered equipment is malfunctioning and that if the registered equipment is determined to be malfunctioning, the use of such equipment shall be discontinued until the problem has been corrected.

(4) Instructions that the user must give notice to the telephone company in accordance with the requirements of Section 68.106."

REPLACEMENT PARTS ORDERING

ORDERING INFORMATION

Motorola maintains parts and service depots and authorized service stations strategically located throughout the country. These facilities are fully equipped to give the finest service. Orders for all parts except crystals, channel elements, "Vibrasender" and "Vibrasponder" resonant reeds, "Permacode" active filters, and "Permacode" Code Plugs should be sent to the nearest parts depot. Orders for instruction manuals should also be sent to the parts depot.

When ordering replacement parts, the complete number identification of the item must be used whether it be a component, kit or complete chassis. This will fix proper identification and assure delivery of the desired item. Complete number identification should also be used when requesting equipment information.

Crystal and channel element orders should specify the crystal or channel element type number, crystal frequency, carrier frequency, and the chassis model number in which the part is used.

Orders for "Vibrasender" and "Vibrasponder" resonant reeds, and "Permacode" active filters should specify the type number and frequency and should identify the owner/operator of the communications system in which these items are to be used.

Orders for programmed "Permacode" Code Plugs should specify desired code.

FACTORY ADDRESS FOR CRYSTAL, CHANNEL ELEMENT, RESONANT REED, AND "PERMACODE" ACTIVE FILTER ORDERS.

AIR MAIL ORDERS

Motorola, Inc.
Component Service Department
P.O. Box 66191
O'Hare International Airport
Chicago, IL 60666

REGULAR MAIL ORDERS AND CORRESPONDENCE

Motorola, Inc.
Component Service Department
2553 Edgington Street
Franklin Park, IL 60131
Tel: 312-451-1297, TWX: 910-227-0799

PARTS DEPOT

Western Parts Dept.

1170 Chess Dr., Foster City,
San Mateo, CA 94404
Tel: 415-349-3111, TWX: 910-375-3877

Pacific Southwestern Area Parts Dept.

P.O. Box 85036, San Diego, CA 92138
Tel: 714-292-8224, TWX: 910-335-1634

Southwestern Parts Dept.

3320 Belt Line Rd., Dallas, TX 75234
Tel: 214-241-2151, TWX: 910-860-5505

Midwest Parts Dept.

10 W. North Ave., Lombard, IL 60148
Tel: 312-620-3000, TWX: 910-693-1592

Communications Div. Parts Dept.

1313 E. Algonquin Rd., Schaumburg, IL 60172
Attn: Communications Division - Parts Dept.
Tel: 312-397-3500, TWX: 910-693-1592
Alternate TWX: 910-693-1599

East Central Parts Dept.

12955 Snow Rd., Parma, OH 44130
Tel: 216-267-2210, TWX: 810-421-8845

Mid-Atlantic Area Parts Dept.

7230 Parkway Dr., Hanover, MD 21076
Tel: 301-796-8600, TWX: 710-862-1941

Eastern Parts Dept.

85 Harristown Rd., Glen Rock, NJ 07452
Tel: 201-447-4000, TWX: 710-988-5602

Southeastern Parts Dept.

P.O. Box 368, Decatur, GA 30031
Tel: 404-981-9800, TWX: 810-766-0876

National Accounts

Federal Government, Railroads, Airlines, and Telephone
1313 E. Algonquin Rd., Schaumburg, IL 60196
Tel: 312-397-3500, TWX: 910-693-1592

Motorola National Data Services

1711 W. 17th St., Tempe, AZ 85281
Tel: 602-994-6472

Radio Paging Terminal